

One-Step Fabrication of High-Performance All-SWNT Field-Effect Transistors by Patterned Growth Technique

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Carbon nanotube field-effect transistor (CNT-FET) is a promising candidate for future electronic devices due to the excellent electronic properties. Recently, FET using CNTs as both electrodes and channel has been demonstrated [1]. The all-CNT devices can work on a flexible substrate without degrading their electrical properties [2,3] and may realize metal-free electronics. The fabrication technique is, however, complicated because it requires multiple CVD steps and I_{ON}/I_{OFF} ratio is so far very low, not comparable with conventional CNT-FETs.

We realized a high-performance all-SWNT FETs with a large I_{ON}/I_{OFF} ratio and excellent transfer characteristics, fabricated by modifying our SAM-based patterning technique [4]. With an improved patterning technique of SAM film, metal catalysts are dip-coated in SAM removed area. By ACCVD technique patterned SWNT are grown on a Si substrate with 50 nm SiO_2 layer. Here, vertically aligned and horizontal SWNTs, acting as electrodes and channel, respectively, are simultaneously synthesized in a one-step CVD process [Fig. 1(a)]. For measuring the FET properties in the back-gated configuration, the vertically-aligned SWNT films were used as source/drain electrodes as shown in Fig. 1(b). The resulting FET transfer characteristics show excellent properties with I_{ON}/I_{OFF} ratio of 10^6 although the fabrication process is very simple. Here, the application of such all-SWNT FET will be discussed.

References

- [1] W. Zhou et al., *J. Am. Chem. Soc.* **132**, 336 (2010).
- [2] Q. Cao et al., *Appl. Phys. Lett.* **88**, 113511 (2006).
- [3] T.Y. Tsai et al., *Appl. Phys. Lett.* **95**, 013107 (2009).
- [4] R. Xiang et al., *J. Am. Chem. Soc.* **131**, 10344 (2009).

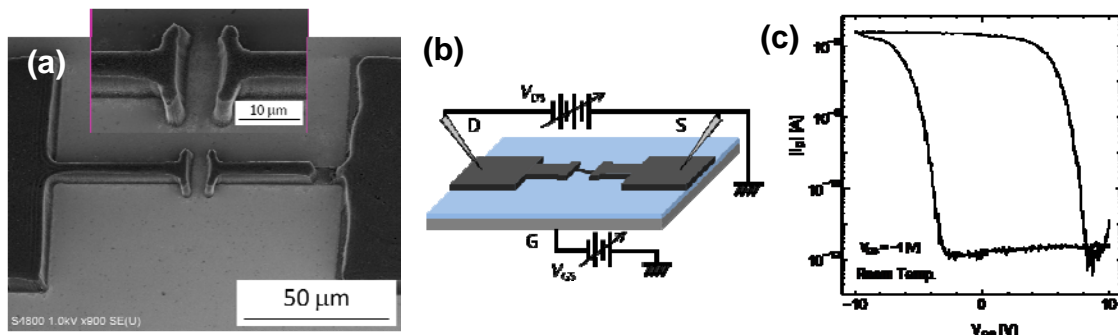


Fig. 1. (a) SEM images of the fabricated all-SWNT FET. The electrode-shape films consisted of vertically aligned SWNTs. The inset shows magnified image of the gap. (b) Schematic of back-gated all-SWNT FET. (c) Transfer characteristics of an all-SWNT FET operated at room temperature. $V_{DS} = -1$ V.