Simple Fabrication Technique for Field-Effect Transistor Array Using As-Grown Single-Walled Carbon Nanotubes

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Abstract

A carbon nanotube field-effect transistor (CNT-FET) is a promising candidate for future electronic devices, however, the fabrication process is still challenging. We propose a simple fabrication technique for CNT-FET arrays using as-grown single-walled CNTs (SWNTs) as the gate channel. In this study, a hydrophobic self-assembled monolayer (SAM) was used to restrict the catalyst-supporting area after fabrication of an electrode array. Since it is known that droplets are trapped at rough edges of a hydrophobic surface, liquid-based catalyst deposition followed by alcohol catalytic CVD produced SWNTs that grew only at the corners of electrode edges. *I-V* characterization of FETs with a 40 μm-channel width showed that 98% of the fabricated devices were electrically connected and more than 50% were functional FETs ($I_{ON}/I_{OFF} > 10^2$). We also investigate the sheet

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resistance of as-synthesized SWNT film.

1. Introduction

A single-walled carbon nanotube (SWNT) is one of the most attractive materials because of its quasi-one-dimensional (1D) structure and chilarity-dependent electronic properties (i.e., metallic or semiconducting). Particularly in the small diameter regime, carrier scattering is suppressed; hence ballistic transport and high carrier mobility (i.e. high-speed operation) can be realized.[1,2] A carbon nanotube field-effect transistor (CNT-FET) with SWNT channel is therefore a promising candidate for future electronic applications. Various types of CNT-FET based devices such as non-volatile memory,[3] optoelectronic emitters,[4] bio sensors,[5] pressure sensors,[6] etc. have been reported. In order to integrate these devices on a chip, position-controlled growth of SWNTs is essential. By using conventional techniques including lithography, metal deposition, and lift-off, SWNTs are locally synthesized for device fabrication.[7,8] Although such processes may work well, many steps are involved and there are limitation on the catalysts that can be deposited using a dry process.

We have recently reported site-selective growth of SWNTs via dip-coating and alcohol catalytic CVD (ACCVD) by controlling the wettability of substrate surface.[9] Because the catalyst solution does not wet a surface functionalized by a hydrophobic self-assembled monolayer (SAM), patterned growth of SWNTs can be obtained. This method is compatible with scalable and cost-effective liquid-based catalyst preparation. Furthermore, development and lift-off processes are not required. This technique is indeed simple, but when there is roughness on the substrate, even if the surface is fully covered by SAM, droplets are trapped there and SWNTs would grow from those rough areas. This phenomenon has been well known as a problem occurring during a Si wafer drying process.[10] In semiconductor production, it has been tried to completely remove water-marks, which the remaining droplets create, by improvement of the drying method and/or by hydrophilicity of the substrate surface.[10-13]

In this study, we focused the “corner effect” mentioned above, which current Si-CMOS processes try to avoid, and realized facile fabrication of FETs using as-grown SWNTs by selective supporting of catalyst at electrode edges. Other than ref. 9, we know of no other reports using a wet process for

local catalyst deposition, which can be useful for CNT-FET fabrication. Here we discuss how catalyst deposits onto the electrode edge, as well as the electrical properties of these as-grown SWNT-FETs synthesized by alcohol CVD. We also investigated the sheet resistance of as-grown SWNTs film, which are formed when the substrate surface is not modified by SAM.

2. Device Fabrication

A thermally oxidized *p*-type Si wafer (t_{ox}: 600 nm) was used as a substrate. The electrode array was firstly patterned on the substrate using photolithography, metal deposition (Pd/Au), and lift-off processes. An optical micrograph of the fabricated array is shown in Fig. 1. The electrode gap for all configurations was fixed at 5 μm. The thicknesses of the Pd and Au layers, which were prepared using a thermal evaporator (ULVAC VPC-260F) with quartz crystal thickness meter (CRTM-6000), were 15 nm and 50 nm, respectively. The substrate with electrodes was subjected to oxygen plasma (100 W, 100 Pa) for ashing organic contaminants, and was then submerged for 15 min in a toluene-octadecyltrichlorosilane (OTS) to form a hydrophobic surface. The volumetric ratio of toluene to OTS is 500 to 1. Dip-coating[14] and ACCVD[15] were performed for SWNTs synthesis. The catalyst was supported at the electrode edge on the substrate, which was dip-coated into a Co acetate solution (0.01 wt% dissolved in ethanol) and was withdrawn slowly. The catalyst was oxidized by annealing the dip-coated substrate in air at 400 °C, and was then reduced in a flowing Ar/H_2 mixture (3% H_2, 300 sccm flow rate, 40 kPa) during heating of the CVD chamber. When the chamber reached 800 °C, the Ar/H_2 flow was stopped and SWNTs were synthesized by supplying ethanol vapor at 1.3 kPa (10 Torr) for 10 min. The details of SWNT synthesis procedures have been described in previous reports.[16-18]

After SWNTs synthesis, the devices were characterized by a semiconductor parameter analyzer system (Agilent 4156C) and scanning electron microscopy (SEM; Hitachi S-4800, acceleration voltage at 1 kV). SEM observation was carried out after measuring the FET properties in order to avoid any damage to the SWNTs by electron irradiation,[19] which could result in an obvious change

in the electronic properties[20]. The Si substrate was used as a back-gate electrode, and all electrical measurements were performed at room temperature under ambient conditions.

3. Results and Discussion

By using a wet process for catalyst preparation (e.g. dip- or spin-coating), a catalyst solution was supported only along the electrode edges as shown in Fig. 2(a). Because droplets do not remain on a super-hydrophobic OTS-SAM surface[9] no SWNT growth is observed in the SAM-covered regions. In contrast, catalyst can be entirely deposited on the surface that has not been functionalized by OTS. The effectiveness of SAM surface coverage by a liquid-based catalyst preparation is shown later. The SEM image shown in Fig. 2(b) clearly indicates that SWNTs were locally grown only from electrode edges. Because OTS-SAM can only form on an OH-terminated surface, the wettability of the electrode surface differs from that of the modified SiO_2 surface. We assume, therefore, that droplets were physically adsorbed at the electrode corner where different surface energies exist, leading to the formation of catalyst regions for SWNT synthesis. A catalyst layer may also be deposited on the electrode, however, it is difficult to obtain SWNTs on a metal substrate,[21,22], thus no growth was observed. This implies that SWNTs were locally grown from the SiO_2 surface only at the electrode edge. It has also been reported that SWNTs can be grown from inactive metals,[23] but if dip-coating is not performed no SWNTs are grown under our experimental conditions, confirming that the deposited Au and Pd for electrodes did not catalyze SWNT synthesis. Therefore, SWNT growth from the electrode edge suggests that catalyst solution was trapped there. While, one possibility is that the catalyst particles attach to the residual resist at the electrode edge and SWNTs were site-selectively grown from the edge, however, since the substrate was carefully washed by hot acetone after lift-off and was also ashed by oxygen plasma before SAM formation, no residual resist should remain. Furthermore, adhesion of catalyst particles on the residual resist is highly unlikely because the resist would dissolve in the ethanol-based dip-coat solution.

Figure 3 shows the *I-V* characteristics of a fabricated device operated at room temperature under

ambient conditions. Typical semiconducting (black dots) and metallic (red dots) properties were shown in the output characteristics (a) and the transfer characteristics (b). The ON-state resistance (R_{ON}) of the semiconducting and metallic devices estimated from Fig. 3(a) are 3.0 MΩ and 240 kΩ, respectively, which are relatively high. In particular, the R_{ON} of the FET with depletable drain current is about 100 times larger than that of the Pd-contacted CNT-FET[24], even though our devices are also Pd-contacted. This might be due to the contact geometry between channel SWNT and the metal electrode. If our devices are end-contacted, the contact resistance should be high, as opposed to the SWNT-embedded configuration, which increases the effective contact area between the channel and the electrode.[25] Another possibility is that the contact between the channel SWNT and the electrode was insufficient because SWNTs were grown from the electrode edge but not on the electrode.

When the channel was composed of a semiconducting SWNT, a device with unipolar *p*-type behavior, for which electrical conductivity is strongly suppressed at positive gate voltages and is highly enhanced at negative gate voltages, is obtained with a large I_{ON}/I_{OFF} ratio of more than 10^6 as shown in Fig. 3(b). While the drain current is independent of the gate voltage, the existence of metallic SWNTs is recognized. From these *I*-*V* characteristics in Fig. 3, it is expected that the gate channel is formed by one or two nanotube contacts between electrodes. We assume that a well-contacted channel among bridging SWNTs forms a conducting path. In fact, although a maximum ON-state current of metallic devices is about six times higher than that of semiconducting FETs, the difference is much lower compared with a thin film channel (shown later).

In order to fabricate a CNT-FET array, we investigate the probability of bridging SWNTs between electrodes with different channel widths of 20 μm and 40 μm (Fig. 1). As shown in Fig. 4, in the case of 20-μm channel width, a drain current (I_D) was detected in 58% of the devices. The remaining 42% of the device was electrically disconnected. However, this does not mean no SWNT were grown between electrodes. We confirmed the existence of SWNTs in the electrode regions.

When the wider electrode (W = 40 μm) was used, the yield achieved as high as 98% among 60 measured devices, however, the I_{on}/I_{off} ratio decreased. This should be attributed to the presence of metallic SWNTs, since the probability of contact between SWNTs and electrode increases.

We analyzed the fabricated devices acting as functional FETs, which means I_D depletes at the positive gate bias (V_{GS}) and the I_{ON}/I_{OFF} ratio is more than 100. Based on this criteria, resultant yields of functional FETs attained were 77% and 52.5% for electrode widths W = 20 μm and 40 μm, respectively. This yield is much better than previous works reporting fabrication of FET arrays using as-grown SWNTs.[26,27] As discussed above, the number of electrically connected devices depended on the electrode shape. Although our devices have the same channel length and width as those in ref. 27, the reason for the higher yield in our case might be due to our lack of post-processing; electrode fabrication after SWNT growth may induce significant damage. Based on this we assume that post-processing-free fabrication methods can achieve higher device yields. Further study is needed to quantify any damage induced by processing after SWNT synthesis.

Finally, we show the effectiveness of using surface wettability to control the catalyst loading using a wet-process, and investigate the sheet resistance of as-grown SWNT thin films. We prepared substrates with and without SAM, and dip- or spin-coated (3000 rpm, 30 s) a catalyst solution onto the substrates. Figure 5 shows SEM images after ACCVD using the substrates prepared under the following conditions: dip-coating with SAM (a), spin-coating with SAM (b), dip-coating without SAM (c), and spin-coating without SAM (d). From these SEM images, we do not find any obvious differences between dip- and spin-coating. However, when the surface was functionalized by OTS-SAM, SWNTs were locally grown from the electrode edge. On the other hand, a SWNT thin film was uniformly grown over the unmodified substrate surface. We measured the sheet resistance by the two-terminal method of the as-grown SWNT thin film formed between electrodes. The resultant resistances are, as shown in Fig. 6, 36.2 kΩ/□ (dip-coat) and 39.2 kΩ/□ (spin-coat), respectively. Even if the contact resistance between SWNT film and metal electrode is

considered, depending on the measurement methods, these values roughly correspond to the in-plane sheet resistance of a vertically-aligned SWNT film (25.9 kΩ/□),[28] which was measured by the four-probe method.

4. Conclusions

We have demonstrated CNT-FETs utilizing as-grown SWNTs can be easily fabricated using a liquid-based catalyst deposition method. SWNTs were found to grow only from the electrode edge after functionalizing the substrate surface using OTS-SAM, followed by catalyst loading by dip- or spin-coating. This was performed after fabrication of the electrode array, eliminating the need for post-processing of the SWNTs. Characterization of the SWNT-FETs showed that, for a channel width of 40 μm, 98% of 60 devices were electrically connected, and more than 50% of these devices worked as functional FETs. The localized catalyst supporting method presented here will provide easy batch fabrication of CNT-FET arrays, and may realize large-scale integration of CNT-FET based devices. We believe that the yield of functional FETs can be increased by optimization of channel width and length,[29] or by plasma-enhanced CVD, which is possible to synthesize quasi-semiconducting SWNTs.[30] It is also expected that the sheet resistance of as-grown SWNT thin film can be easily characterized since SWNTs were uniformly grown on the substrate when SAM was not used.

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Figure captions

Fig. 1. Optical micrograph of fabricated device array. Electrodes having channel widths of 20 μm and 40 μm were used in this study.

Fig. 2. (a) Schematic diagram of the possible catalyst deposition mechanism. (b) A typical SEM image after CVD shows SWNTs were selectively grown from the electrode edge.

Fig. 3. Electrical properties of semiconducting (black) and metallic (red) devices. All back-gated FETs were operated at room temperature under ambient conditions. (a) Output characteristics, V_{DS} and V_{GS} were applied from 0 V to −15 V and +10 V to −10 V with a −2 V step in both cases. (b) Transfer characteristics at V_{DS} = −10 V.

Fig. 4. I_{ON}/I_{OFF} distribution of FETs with different channel widths. The yield achieved as high as 58% (W = 20 μm) and 98% (W = 40 μm), respectively, among 60 measured devices.

Fig. 5. SEM images after SWNT synthesis on substrates prepared under different conditions: (a) dip-coating with SAM; (b) spin-coating with SAM; (c) dip-coating without SAM; (d) spin-coating without SAM. Scale bars are 10 μm.

Fig. 6. The sheet resistance of as-grown SWNT thin films prepared by dip-coating (black) and spin-coating (red).

Figures

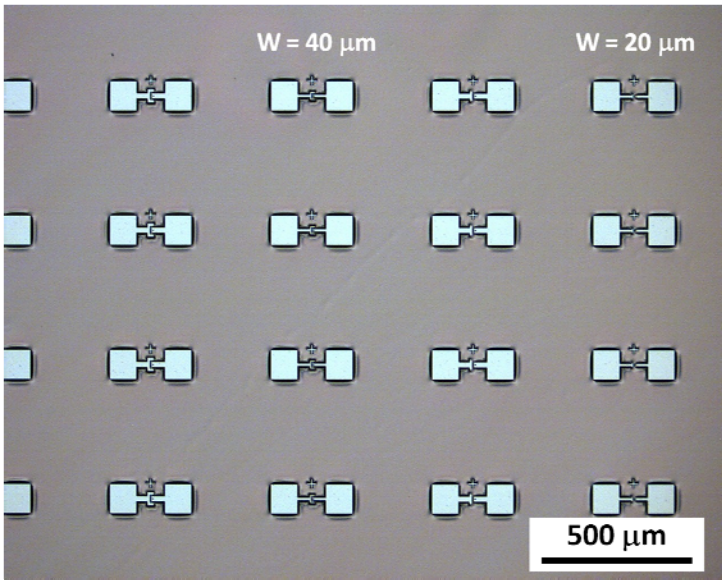

Fig. 1

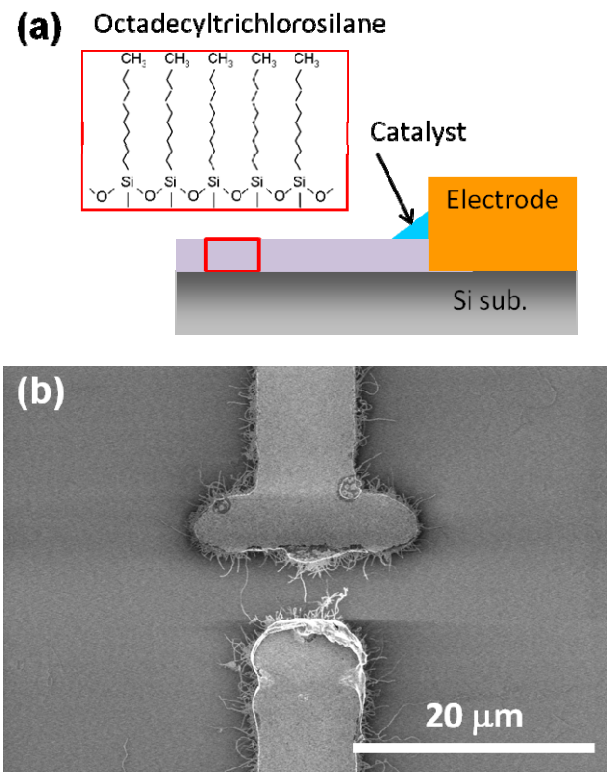
(a)
Octadecyltrichlorosilane
Catalyst
Electrode
Si sub.
(b)
20 μm

Fig. 2

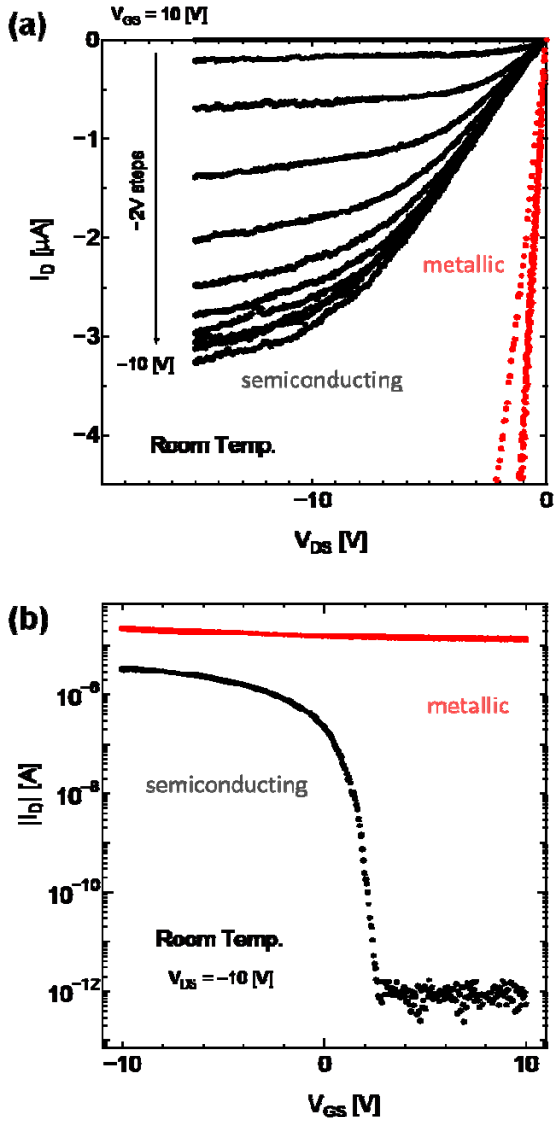
(a)
V_{GS} = 10 [V]
0
−1
−2
−3
−4
I_D [μA]
−2V steps
−10 [V]
metallic
semiconducting
Room Temp.
−10
0
V_{DS} [V]
(b)
10^{-6}
10^{-8}
10^{-10}
10^{-12}
$|I_D|$ [A]
metallic
semiconducting
Room Temp.
V_{DS} = −10 [V]
−10
0
10
V_{GS} [V]

Fig. 3

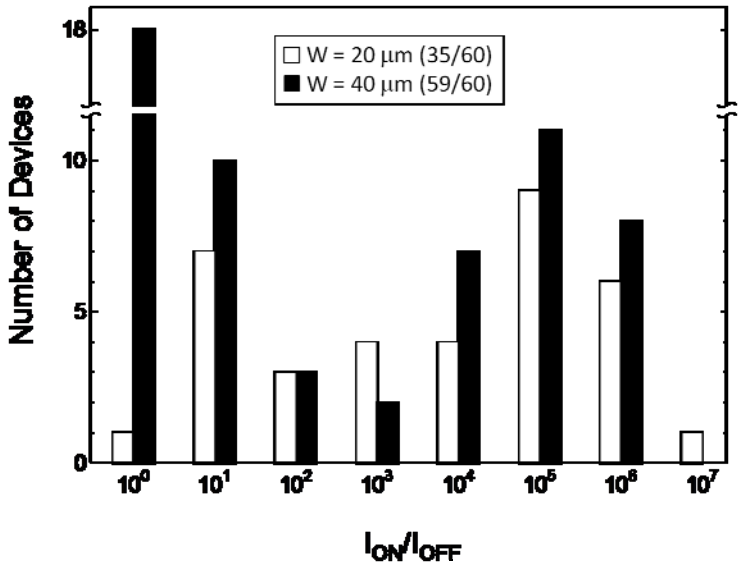
W = 20 μm (35/60)
W = 40 μm (59/60)
Number of Devices
18
10
5
0
10^0
10^1
10^2
10^3
10^4
10^5
10^6
10^7
I_ON/I_OFF

Fig. 4

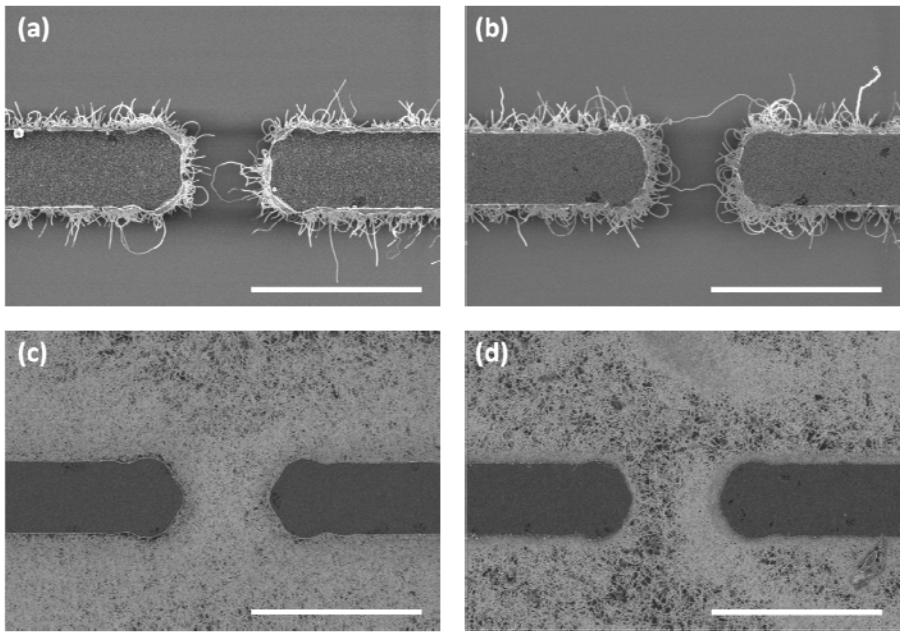

Fig. 5

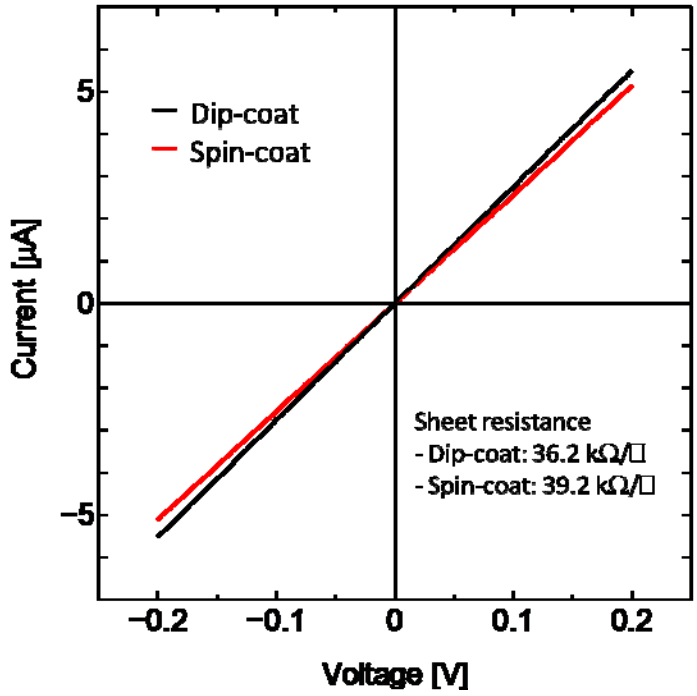
Dip-coat
Spin-coat
Current [μA]
Voltage [V]
5
0
−5
−0.2
−0.1
0
0.1
0.2
Sheet resistance
- Dip-coat: 36.2 kΩ/□
- Spin-coat: 39.2 kΩ/□

Fig. 6