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Abstract Details

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Abstract

TITLE: Patterned CVD Growth of Single-Walled Carbon Nanotubes for a Thin-Film Transistor

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ABSTRACT BODY: Two different patterned growth techniques of single-walled carbon nanotubes (SWNTs) based on dip-coating catalyst-loading process and alcohol CVD (ACCDV) method [1] are explored for a simple manufacturing of thin-film nanotube transistor. The first approach is the conventional concept of using SiO_2 patterned Si substrates. Using a dip-coating method [2] followd by alcohol CVD growth, high-quality vertically aligned SWNTs (VA-SWNT) [3,4] patterns can be easily obtained. This results the 3D carbon nanotube structures [5]. Apart from the sintering of catalyst into Si at high temperature, the difference in surface wettability between Si and SiO_2 also plays an important role in this selective growth, which leads us to a novel method of patterning the growth on chemically modified surfaces. The more elaborate and precise patterned growth is based on the controll of wettability of substates [6]. Surface wettability strongly affects the deposition of catalyst in dip-coating process. By functionalizing the silicon surface using a conventional self-assembled monolayer (SAM) and then selectively removing the SAM by ultraviolet (UV) light, the catalyst can be dip-coated onto only the hydrophilic areas of the substrate. This method can simplify fabrication without sacrificing the resolution in the case of using conventional UV photolithography. Furthermore, by utilizing an electron beam instead of UV, the line width of an SWNT pattern can be easily reduced to 50 nm. Since the electron beam strength of magnified imaging in scanning electron microscope (SEM) is just enough for this SAM removal, patterned region can be easily located and visualized under a SEM [6]. Employing this pattering method, we fabricated a CNT-FET with an as-grown SWNT as its gate channel and as Si substrate as a back-gate. The I-V characteristics for various devices will be discussed.

References:
[1] S. Maruyama, R. Kojima, Y. Miyauchi, S. Chiashi and M. Kohno, Chem. Phys. Lett., 360 (2002) 229.
[2] Y. Murakami, Y. Miyauchi, S. Chiashi and S. Maruyama, Chem. Phys. Lett., 377 (2003) 49.
[3] Y. Murakami, S. Chiashi, Y. Miyauchi, M. Hu, M. Ogura, T. Okubo, S. Maruyama, Chem. Phys. Lett., 385 (2004) 298.
[4] S. Maruyama, E. Einarsson, Y. Murakami and T. Edamura, Chem. Phys. Lett., 403 (2005) 320.
[5] R. Xiang, E. Einarsson, H. Okabe, S. Chiashi, J. Shiomi, Jpn. J. Appl. Phys., (2009), in press.
[6] R. Xiang, T. Wu, E. Einarsson, Y. Suzuki, Y. Murakami, J. Shiomi, S. Maruyama, J. Am. Chem. Soc., 131 (2009) 10344.

(No Table Selected)