On-chip sorting of long semiconducting carbon nanotubes for multiple transistors along an identical array

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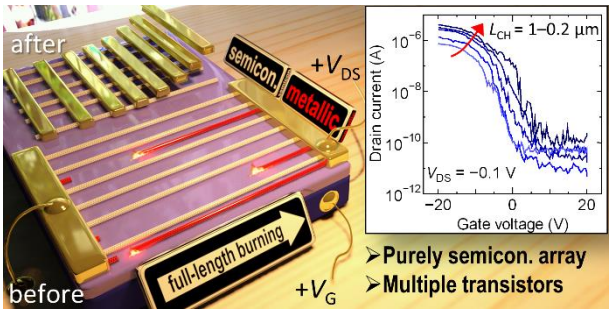
ABSTRACT

Ballistic transport and sub-10 nm channel lengths have been achieved in transistors containing one single-walled carbon nanotube (SWNT). To fill the gap between single-tube transistors and high-performance logic circuits for the replacement of silicon, large-area, high-density, and purely semiconducting (s-) SWNT arrays are highly desired. Here we demonstrate the fabrication of multiple transistors along a purely semiconducting SWNT array via an on-chip purification method. Water- and polymer-assisted burning from site-controlled nanogaps is developed for the reliable full-length removal of metallic SWNTs with the damage to s-SWNTs minimized even in high-density arrays. All the transistors with various channel lengths show large on-state current and excellent switching behavior in the off-state. Since our method potentially provides pure s-SWNT arrays over a large area with negligible damage, numerous transistors with arbitrary dimensions could be fabricated using a conventional semiconductor process, leading to SWNT-based logic, high-speed communication, and other next-generation electronic devices.

KEYWORDS: carbon nanotube, aligned array, purification, field-effect transistor, electrical burning

TOC graphic



Bulk-silicon field-effect transistors will not work reliably at ultrascaled gate lengths, such as less than 10 nm.[1] One possible way to continue the scaling of transistors is to change the channel geometry and/or materials for better electrostatic control. The extraordinary electrical properties and ultrathin bodies of semiconducting single-walled carbon nanotubes (s-SWNTs) make them attractive for use in logic transistors and optoelectronic devices.[2–7] A horizontal array configuration is desirable to realize optimal use of the excellent properties,[8] while the coexistence of metallic (m-) SWNTs causes excessive leakage from transistors in the off-state. Although an aligned assembly of s-SWNTs after liquid-phase separation has been developed,[3,5] the lengths and degree of alignment has room for improvement. Another means to obtain high-purity s-SWNT arrays is direct chemical vapor deposition (CVD) growth on single-crystal substrates, which provides high-density SWNT arrays over a large area.[9–11] Chirality-controlled growth, which has undergone considerable progress in recent years,[12,13] has not realized sufficient purities of s-SWNTs; therefore, on-chip purification methods are still required. Some approaches exploit the leak current (Joule self-heating) in m-SWNTs by the application of a high bias voltage.[14–17] Toward the fabrication of pure s-SWNT arrays over a large area, nanoscale trenches formed through thermocapillary flows in organic resists have been used to etch the exposed m-SWNTs in full length,[15,16] but the relatively large width of the trenches (>100 nm) limits the applicability of such methods to high-density arrays. In addition, there have been no reports on the fabrication of multiple transistors from a long s-SWNT array.

Recently, we reported that horizontally aligned m-SWNTs keep burning in a self-sustainable manner (over >10 μm long) once ignited via voltage application with the

assistance of water vapor and polymer coating,[18,19] where the water drastically increases an oxidation rate of SWNTs and the polymer supplies heat to the SWNTs though its oxidation. However, the electrical burning was found to propagate only in one direction from random breaking points, which hindered the full-length removal of m-SWNTs and thus the fabrication of purely s-SWNT arrays. This one-way burning is triggered at the nanogaps by field emission and water-mediated electrochemical etching[20] rather than by Joule self-heating, leaving a chance for improvement of the process.

In this work, we present a method for the full-length burning of m-SWNTs by overcoming the problem with water- and polymer-assisted (WPA) burning. Since the gap formation process and subsequent burning process can be separated, full-length burning is achieved after nanogaps in m-SWNTs are formed in a small controlled area. We have successfully fabricated multiple transistors along the resultant s-SWNT array, and demonstrate large on-state conductance and superb switching behavior in the off-state (on/off ratio ~10^5) for all devices with various dimensions. WPA burning from the pre-formed nanogaps lowers the voltage required to initiate burning, which reduces the damage to s-SWNTs through the sorting. Toward the use in high-performance applications, the upper limit of the SWNT density is discussed to which the selective burning technique can be applied without damaging neighboring s-SWNTs.

RESULTS AND DISCUSSION

1. On-chip sorting of s-SWNT arrays

Figures 1a-d show the purification procedures for the full-length burning of m-SWNTs. Third (middle) Au contacts, as well as two (top and bottom) contacts, were patterned on the SWNT arrays (Figure 1a) to form nanogaps in the vicinity of the bottom metal contacts, to which a lower potential was applied (cathode). A corresponding scanning electron microscopy (SEM) image is shown in Figure 1e. Electrical breakdown of the SWNTs was performed to create nanogaps between the middle and bottom contacts. After the middle metal contacts were selectively etched away, eight nanogaps in the m-SWNTs were produced beside the bottom contacts, as indicated by the red circles in Figure 1f. The transfer characteristics of the transistor defined by the middle and bottom (source and drain) contacts indicate that all the m-SWNTs were broken down, as shown by the red curve in Figure 1h. The reduction of the on-state current after the removal of middle contacts (Figure 1h, blue curve) is simply attributed to the change in the channel length L_{CH}, from ~2 to ~10 μm.

WPA burning[19] from nanogaps was utilized to remove remaining m-SWNTs. The SWNT arrays (Figure 1f) were embedded in poly(methyl methacrylate) (PMMA) thin films. A ramp voltage (up to 35 V) was then applied to the SWNT arrays in a wet oxygen environment. Figure 1g shows an SEM image of the SWNT arrays after m-SWNT burning from site-controlled nanogaps and removal of the PMMA thin film with acetone. Since burning from nanogaps occurs in the SWNTs connected to the metal contact to which a higher potential is applied (anode), SWNT fragments at the anode side of the nanogaps were completely burned out. Thus, almost full lengths of the m-SWNTs were removed, except for very short fragments in the designated area close to the bottom contact, and therefore a purely semiconducting SWNT array was obtained in the selected area. During the sorting of s-

SWNTs, SWNTs can be kept very clean because only PMMA, Au, and photoresists, which can be easily removed,[21,22] are in direct contact with the SWNTs.

The atomic force microscopy image in Figure S2 in the Supporting Information (SI) shows the residues thinner than the original SWNTs after the SWNTs were burned from the nanogaps. Several metal contacts were placed on the burned m-SWNT area, which confirmed that this type of thin residue from the m-SWNT was not conductive, as shown in Figure S3.

Note that the purification process that involves the pre-formation of nanogaps caused little damage to the s-SWNTs. In the first electrical breakdown process to form nanogaps, most of the SWNTs, which are embedded in Au contacts, were not subjected to a high electric field. Even if s-SWNTs are damaged during the gap formation, the damage is controlled in the small area which is not used for the fabrication of transistors. In the subsequent burning process, the on-state current of the transistor defined by the top and bottom (source and drain) contacts did not decrease as shown by the blue and green curves in Figure 1h. This is because the burning from pre-formed nanogaps can be triggered by the application of a low voltage (35 V), which is much lower than the electrical breakdown.

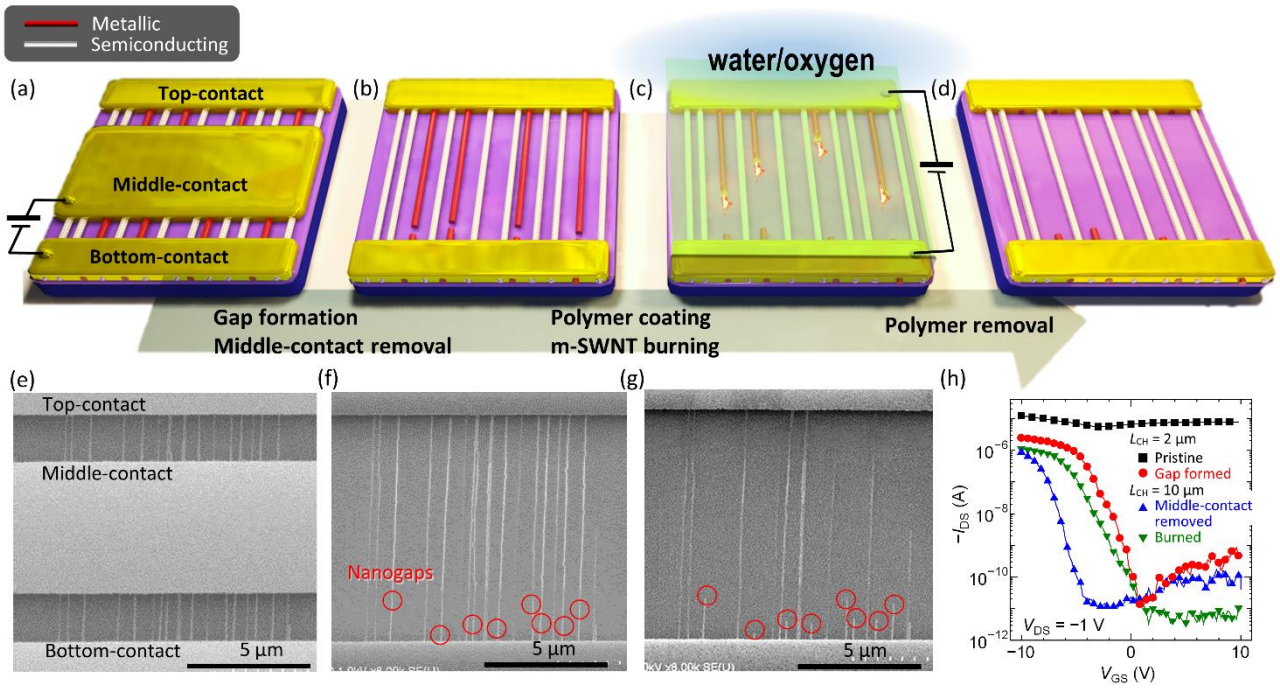


Figure 1 (a-d) Schematics for full-length removal of m-SWNTs in a controlled area. (e-g) SEM images of SWNT arrays corresponding to (a), (b), and (d). (a,e) Initial SWNT arrays with three (top, middle, and bottom) metal contacts. A ramp voltage (V_{DS}) was then applied between the middle and bottom contacts until all the m-SWNTs were broken down. (b,f) After electrical breakdown, the middle contacts were dissolved to leave SWNT nanogaps (red circles) close to the bottom contacts. (c) After PMMA was coated onto the substrate, another ramp voltage was applied in a wet oxygen environment. All the m-SWNTs were then burned from the nanogaps in one direction. (d,g) After burning, only the s-SWNTs remained. (h) Transfer characteristics of the transistor defined by the middle and bottom contacts, before and after formation of the nanogaps (black and red, respectively), after removal of the middle contact (blue), and after burning (green).

2. Fabrication of multiple transistors along the s-SWNT array

Since a purely s-SWNT array was obtained over an area of 9.9×7.6 μm^2; multiple transistors could be fabricated from the s-SWNTs, as schematically shown in Figures 2a-c. After dissolving the entire Au layer (Figure 2b), a row of metal contacts was patterned by electron beam lithography and thermal evaporation of Ti/Au (Figure 2c). Finally, the devices were annealed at 230 °C in air for 1 h to improve the contact between the SWNTs and the metal. Figure 2d shows a false-colored SEM image of fabricated transistors with various channel lengths (200–960 nm).

Figure 2e shows the transfer characteristics of five transistors on the same SWNT array. All the characteristics show superb switching behavior, which confirms that no m-SWNTs remained in the region where the transistors were fabricated. Figure 2f shows that the on-state current I_{ON} increased linearly with a reduction in the channel length, while the on/off ratio I_{ON}/I_{OFF} remained almost constant (~10^5). This indicates that the s-SWNT array was identical and thus uniform. The identity of SWNT arrays along the axis will reduce the undesirable variations of chiralities and local SWNT density, leading to reliable operation of the SWNT-based circuits.[23] There are nine s-SWNTs in the channel, so that the averaged conductance of each s-SWNT was 4.6 μS, which is the same order as that of previously reported devices with a single as-grown s-SWNT and similar dimensions[2] (see also Figure S4). This can be improved by further vaporizing the PMMA residue before patterning of the metal contacts. It should be stressed that although only five transistors were fabricated in this experiment due to the constraint of measurement and device structure, the number of

transistors fabricated on the s-SWNT array could be increased further by reducing the device dimensions, as long as the lithography process and gate control works. This method will therefore enable device integration with ultrasmall channel/contact length and freedom of circuit design in contrast to the electrical breakdown method.[24]

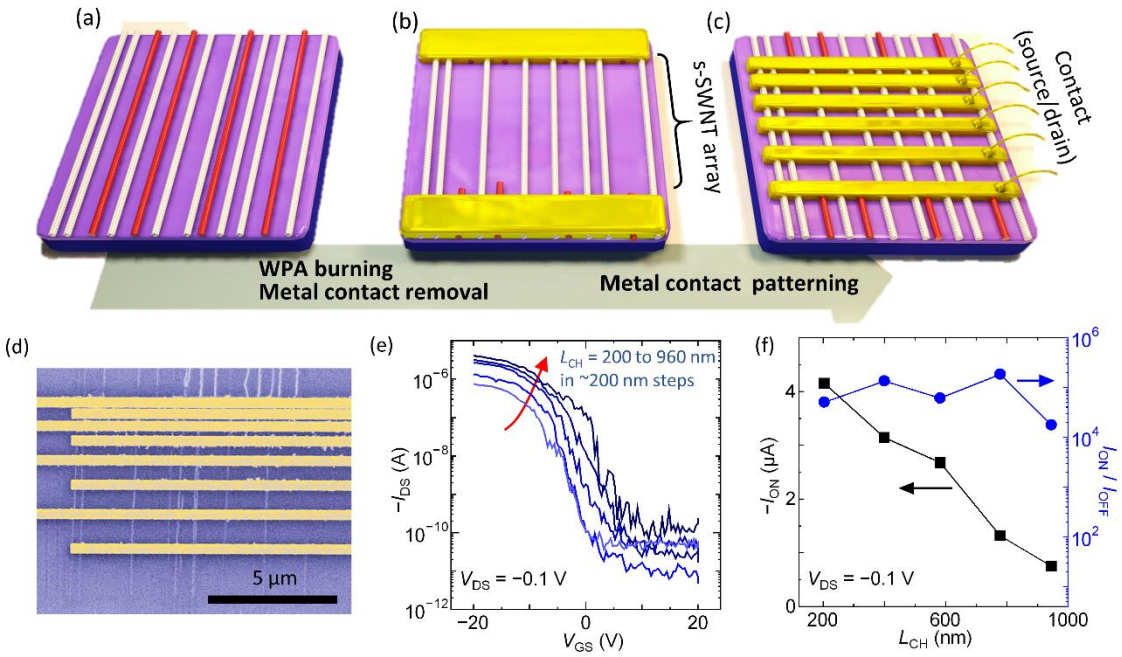


Figure 2 (a-c) Schematics for the fabrication of multiple transistors from the sorted s-SWNT array. (a) Before and (b) after the m-SWNT removal procedure. (c) Schematic and (d) false-colored SEM image of the transistor array fabricated from the s-SWNT array. (e) Transfer characteristics of five transistors with different channel lengths. (f) On current I_{ON} (left axis), and on/off ratio I_{ON}/I_{OFF} (right axis), as a function of the channel length, L_{CH}. V_{DS} = -0.1 V.

The characteristics of transistors built along the s-SWNT array confirmed the elimination of m-SWNTs. For further characterization, we performed the Raman measurement of the SWNT array after the sorting and the deposition of metal contacts using the excitation wavelength of 532 nm. In Figure 3a, Raman mapping of G-band is superimposed on the SEM image of the SWNT array. Since the number of SWNTs was decreased, the purified region had less G-band peaks than the unpurified region on the top. All the Raman spectra obtained in line from the purified region indicated by a red arrow and the unpurified region indicated by a black arrow are plotted in Figure 3b. Though the intensity is different because a part of the s-SWNTs within the laser spot was embedded in metal contacts, the averaged and normalized spectra shown in the inset are almost identical. This indicates that the sorting process induced no change detectable by Raman spectroscopy.

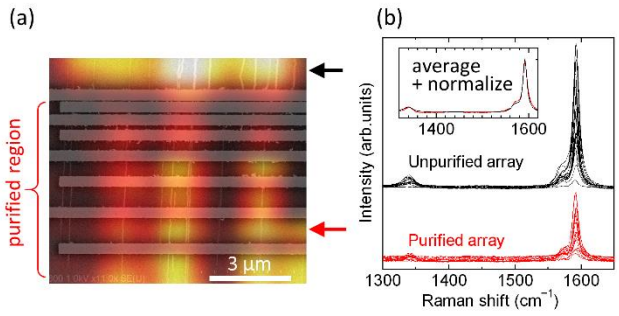


Figure 3 (a) Raman mapping of G-band intensity (1550–1620 cm^{-1}) from the SWNT transistor array shown in Figure 2d. The area above horizontal electrodes was not subjected to the purification process and contained m-SWNTs. (b) Raman spectra obtained from the region between two electrodes indicated by a red arrow and the horizontal region indicated by a

black arrow. Inset: averaged and normalized G-band spectra of the purified (red) and unpurified (black) SWNTs.

3. Comparison of WPA burning and electrical breakdown

We intentionally removed half-lengths of m-SWNTs, and prepared both purified and unpurified SWNT arrays from the same set of long SWNTs, as shown in Figures 4a and b. Since the unpurified SWNT array was not subjected to any voltage treatment, the effect of the purification process on the SWNTs could be directly evaluated by the fabrication and characterization of transistors with the exact same dimensions on purified and unpurified arrays.

In Figure 4c, transistors on the unpurified array (black curves) show typical characteristics of short circuits caused by m-SWNT impurities, while those on the purified array (red curves) reflect purely semiconducting behavior. Therefore, the purification process increased the on/off ratio from <10 to ~10^4, as shown in Figure 4d. From the data points with L_{CH} = 200 nm in Figure 4e, the reduction in the on-state current induced by the sorting of s-SWNTs corresponds to only 70%, which is quite modest considering that m-SWNTs conduct more current than s-SWNTs.[25] In both types of transistors, the on-state current was increased with a reduction in the channel length because the SWNT arrays were uniform along the axis.

We performed conventional electrical breakdown[14] for individual transistors on unpurified arrays for comparison with those obtained via full-length WPA burning. All the

transistors tested here were composed of the same set of SWNTs. The electrical breakdown method has shown its applicability in the fabrication of digital systems using CVD-grown SWNT arrays by combining design and processing,[26] even when the SWNT density exceeds 100 tubes/μm.[22] However, the method is quite sensitive to channel length and is expected to fail in ultrascaled devices.[27] A ramp voltage (V_{DS}) was applied to the transistors on the unpurified array until the on/off ratio reached 10^3, while s-SWNTs were turned off by gate. For the longer channel devices ($L_{CH} \geq 600$ nm), on-state current retention was comparable for both the WPA burned devices and the electrical breakdown devices, as shown in Figure 4e. On the other hand, the on-state current was significantly degraded when the channel was scaled further ($L_{CH} \leq 400$ nm). Therefore, our fabrication procedure, where m-SWNTs are completely removed from long SWNT arrays and then source and drain contacts are defined on the semiconducting arrays, is more beneficial than conventional electrical breakdown for a reduction in device dimensions without sacrifice of the on-state current.

The large degradation of the on-state current by electrical breakdown can be explained in terms of heat dissipation and electrostatic problems at the gate. First, a higher electric field (V_{DS}/L_{CH}) is required to cut shorter SWNTs (Figure 4f) because axial heat sinking to metal contacts, rather than to the substrate below, becomes predominant for short-channel devices[28] (see also Figure 5b). This increases the off-state current in s-SWNTs significantly by the time the m-SWNTs are broken down. Second, gate control becomes weak as the channel is scaled due to so-called short-channel effects. The off-state current is increased because of this effect, even at the same voltage. These two effects reduce the difference in the breakdown voltage of s- and m-SWNTs (Figure 4f, right-hand axis), which

restricts the use of the electrical breakdown method in scaled devices. Note that the present devices were not optimized in terms of gate electrostatic, and have much room for reduction of the off-state current in s-SWNTs during the electrical breakdown process.

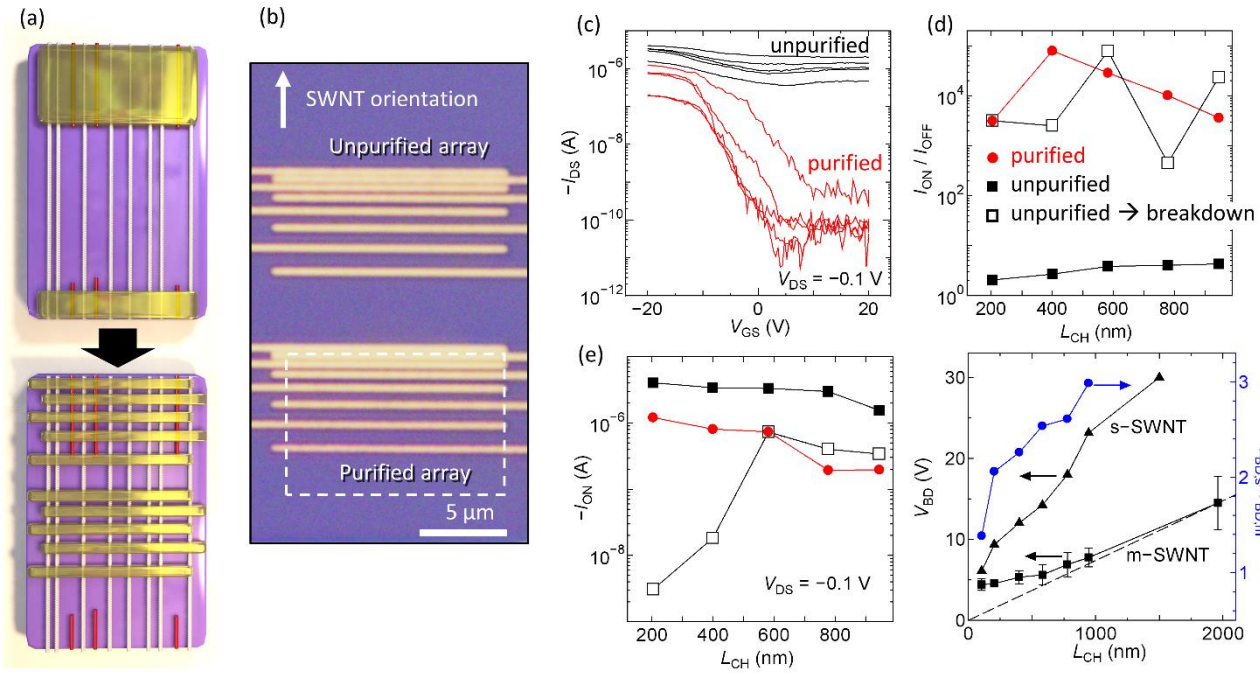


Figure 4 Comparison between transistors fabricated from purified and unpurified SWNT arrays. (a) Schematic for the preparation of purified and unpurified arrays originally from identical SWNTs. (b) Optical image of two transistor arrays fabricated along purified (bottom) and unpurified (top) SWNT arrays. (c) Transfer characteristics of the transistors fabricated from purified (red) and unpurified (black) arrays. (d) On/off ratio I_{ON}/I_{OFF} for the transistors on the purified array (red circles) as a function of the channel length L_{CH}. Plots for the transistors before and after electrical breakdown of the transistors fabricated from the unpurified array (black and open squares, respectively). (e) Similar set of plots for channel length L_{CH} vs. on current I_{ON}. (f) Channel length L_{CH} vs. breakdown voltage V_{BD} for both m- and s-SWNTs. V_{BD} ratio of s- to m-SWNTs is plotted on the right-hand axis.

4. Lengths needed for selective formation of nanogaps

A previous study[19] has shown that polymer coating and introduction of water vapor in the environment did not affect the breakdown voltage/power of SWNTs, but continuous degradation of the conductance which did not obviously appear as electrical breakdown have not been discussed. Various biases V_{DS} were repeatedly applied in a stepwise manner to single s-SWNTs under several conditions while the s-SWNTs were turned off by the gate. The on-state conductance at V_{DS} = -1 V was recorded after each bias application. As shown in Figure 5c, the conductance was gradually decreased after a large V_{DS} (>5 V/μm) was applied, especially for the s-SWNTs in the PMMA films perhaps due to the functionalization of SWNTs induced by high-energy carriers.[29] In the presented purification method, this sort of damage to s-SWNTs was successfully avoided because the voltage required to initiate the burning of m-SWNTs from pre-formed nanogaps (35 V in Figure 1) was much lower than that to burn m-SWNTs of the same length directly by Joule self-heating (~70 V for 10-μm-SWNTs, see Figure 4f). Therefore, the selectivity for the removal of s- or m-SWNTs is dominated by the initial electrical breakdown to form nanogaps. This indicates the purity of final s-SWNTs can be almost high enough for logic applications (>99.9999%) by combining the selective growth with this post-growth sorting.[12,23]

For reducing the size of pre-formed nanogaps and the wasted area where both s- and m-SWNTs remain after the purification, shorter channels should be used for the nanogap formation process while preserving as many s-SWNTs as possible. When an identical m-SWNT partially embedded in metal contacts with a variety of spacing (that is, L_{CH}) is

uniformly heated via Joule self-heating as shown in Figure 5a, the temperature profile along the tube axis for L_{CH} = 1.5 μm or more is calculated[30] to be uniform in the middle (Figure 5b), and is not affected by heat dissipation to the metal contacts. Note that the thermal conductivity of SWNTs was assumed to be 1,000 W/mK, and heat sinking coefficient to the substrates (g = 0.054 W/mK) was estimated from the experiment shown in Figure 1. In addition, the on-state conductance of single-tube transistors built on an identical s-SWNT dropped in prior to the breakdown when $L_{CH} \leq$ 600 nm (Figure 5d). Since shorter SWNTs were subjected to higher electric field when they reached at a breakdown temperature (typically ~600 °C) due to strong heat sinking to metal contacts, the gentle damage to s-SWNTs is likely to be induced by the field rather than thermally induced reaction.

Therefore, the selectivity of removal between s- and m-SWNTs is sufficiently high for devices with $L_{CH} \geq$ 1.5 μm, which is also clear from the breakdown voltage V_{BD} close to a linear dashed line shown in Figure 4f. To further scale up the purification process and reduce the area ratio of unpurified to purified arrays, the distance between anodes and cathodes for the burning process should be increased while all SWNTs are kept connected to both metal contacts. The voltage required to trigger the burning is independent of the SWNT length due to field localization within the nanogaps, and thus the purification process is upscalable without suffering from breakdown of the gate dielectric. In that sense, the growth of long SWNTs is a key for further improvement of the process because the proposed SWNT burning model suggests self-sustained burning without a limit of length.[19]

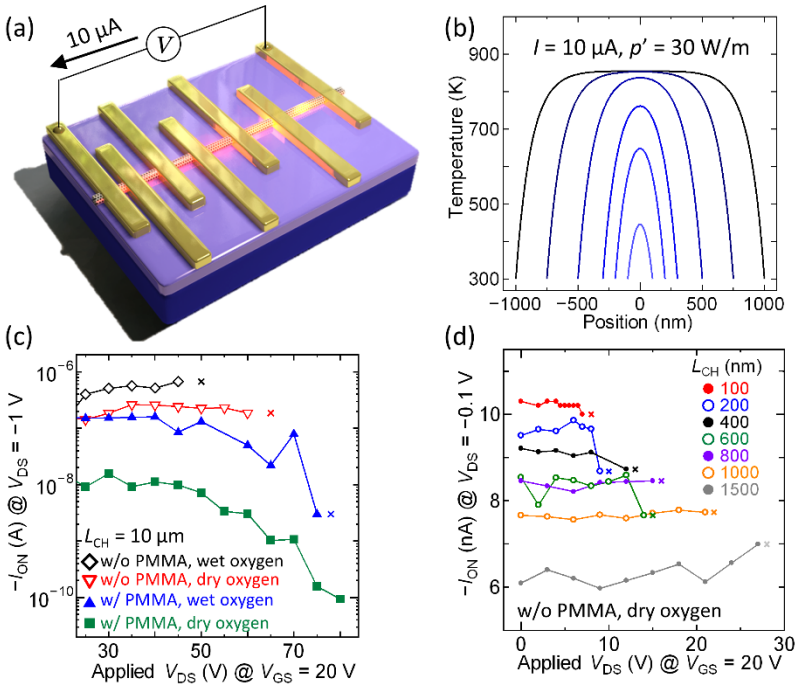


Figure 5 (a) Schematic for the analyzed SWNT device with various channel lengths. SWNTs are heated by uniform Joule self-heating along the axis. (b) Analytical temperature profiles of SWNTs of various lengths (200–2000 nm).[30] (c) Transition of on-state current in single s-SWNT transistors embedded under various conditions (with or without PMMA coating, gas environments). Crossed marks represent the breakdown of SWNTs during next voltage application. L_{CH} = 10 μm. (d) Similar data obtained in dry oxygen without PMMA coating for the transistors with different channel lengths.

5. Consideration on inter-tube spacing and damages

When this technique is applied to high-density SWNT arrays, deterioration of the selectivity caused by inter-SWNT interaction, i.e., the influence of burning SWNTs on neighboring SWNTs, should also be considered. There are two conceivable ways of damage to intact s-SWNTs: voltage-induced tip-to-wall etching and wall-to-wall spreading of chemical reaction via PMMA. We examined the minimum inter-SWNT spacing for which m-SWNTs burned from nanogaps and caused no damage to neighboring s-SWNTs, and the results are shown in Figure 6a. With respect to the first type of damage, the experimental result shows that an s-SWNT 60 nm away from the tip of a broken m-SWNT did not burn out, even when 50 V was applied to burn the m-SWNT (Figures 6a, bottom). In addition, the burning of the m-SWNT did not propagate to the s-SWNT when the minimum inter-SWNT distance was as small as 40 nm (Figures 6a, top).

In contrast, when a nanogap was located close to the anode, an s-SWNT 120 nm away from the nanogap was burned away, even with application of a smaller voltage (40 V), as shown in Figure 6b. This is because the difference in the electric potential between the m-SWNT tip and the s-SWNT wall was greater, as schematically shown in Figure 6c. This implies that burning from site-controlled nanogaps close to the cathode is also beneficial to avoid unintentional damage to neighboring s-SWNTs, and is thus applicable to higher-density SWNT arrays.

Upon the assumption that the burning from nanogaps is triggered by field emission and anode etching due to field enhancement at the SWNT tip, we roughly estimated the upper limit of the density of SWNTs to which this purification method can be applied without

sacrificing s-SWNTs. By ignoring the difference of field enhancement between tip-to-tip and tip-to-wall configurations for simplicity, the field enhancement factor γ at SWNT tips can be expressed in a similar manner to a previous study[20] about the field enhancement on substrates as below (see also Figure S5a-c),

$$\gamma = c\left(1+\sqrt{\frac{2L_{\mathrm{cathode}}}{4r}}\right)\left(1+a\frac{2L_{\mathrm{cathode}}+s_{inter}}{s_{\mathrm{inter}}}-b\frac{s_{\mathrm{inter}}}{2L_{\mathrm{cathode}}+S_{inter}}\right), \qquad (1)$$

where a, b, and c are constants and taken from the previous study,[20] L_{cathode} is the length of broken m-SWNTs connected to the cathode, s_{inter} is the inter-tube spacing, and r is a tube radius. Since the electric potential of unbroken s-SWNTs has a gradient along the axis, the voltage difference V_{inter} between the tip of anode m-SWNTs and the wall of the other side of s-SWNTs is written as $V_{\mathrm{inter}} = V_{\mathrm{DS}}L_{\mathrm{cathode}}/L_{\mathrm{CH}}$. If the threshold field at the SWNT tips for initiating the burning is constant ($F_{\mathrm{th}} = \gamma V_{\mathrm{inter}}/(2L_{\mathrm{cathode}}+s_{\mathrm{inter}})$) and can be estimated from the burning occurring at tip-to-tip, where typically ~30 V was necessary to burn m-SWNTs from 70-nm-nanogaps (Figure S5d), we obtained the threshold voltage that causes the m-SWNT-induced burning of s-SWNTs ($V_{\mathrm{s\text{-}burn}}$) as below,

$$V_{\mathrm{s-burn}}(L_{\mathrm{cathode}}, s_{\mathrm{inter}}) = \frac{F_{\mathrm{th}}(2L_{\mathrm{cathode}}+s_{\mathrm{inter}})}{\gamma}\times\frac{L_{\mathrm{CH}}}{L_{\mathrm{cathode}}}. \qquad (2)$$

Figure 6d shows a color contour plot of the voltage calculated by Eq. (2) when the L_{CH} for the burning process is 10 μm (similar to Figure 1). The examples of the nanogaps shown in Figure 6a and b are plotted as a blue triangle ($V_{\mathrm{s\text{-}burn}} \approx 67$ V > $V_{\mathrm{DS}} = 50$ V) and a red square ($V_{\mathrm{s\text{-}burn}} \approx 32$ V < $V_{\mathrm{DS}} = 40$ V), respectively, which suggests this simple modeling is

consistent with the experimental results. V_{DS} for triggering the m-SWNT burning has to be smaller than $V_{s\text{-}burn}$ to avoid the undesirable removal of s-SWNTs. Since we can reduce the channel length for the first nanogap formation process down to 1.5 μm while keeping the selectivity of breaking m-SWNTs high enough, the inter-tube spacing can be reduced to ~10 nm without sacrificing s-SWNTs under the application of V_{DS} = 35 V (a dashed line in Figure 6d). This implies the sorting method of s-SWNTs could effectively work for the SWNT arrays with density up to ~100 SWNTs/μm owing to the control of gap position. Note that we assumed that ~70-nm-nanogaps are formed by breaking 99.99% (within four standard deviations) of m-SWNTs with V_{DS} = 20 V, and then the m-SWNTs are burned by the further application of V_{DS} = 35 V (as in Figure 1). Scaling up of the purification process (which corresponds to larger L_{CH} in Eq. 2)) is also beneficial in further reducing the inter-tube spacing. Therefore, the sorting method in combination with selective growth of long and high-density s-SWNT arrays[10,11,31] opens the possibility of the practical use of SWNT transistors in large-scale and high-performance logic circuits.

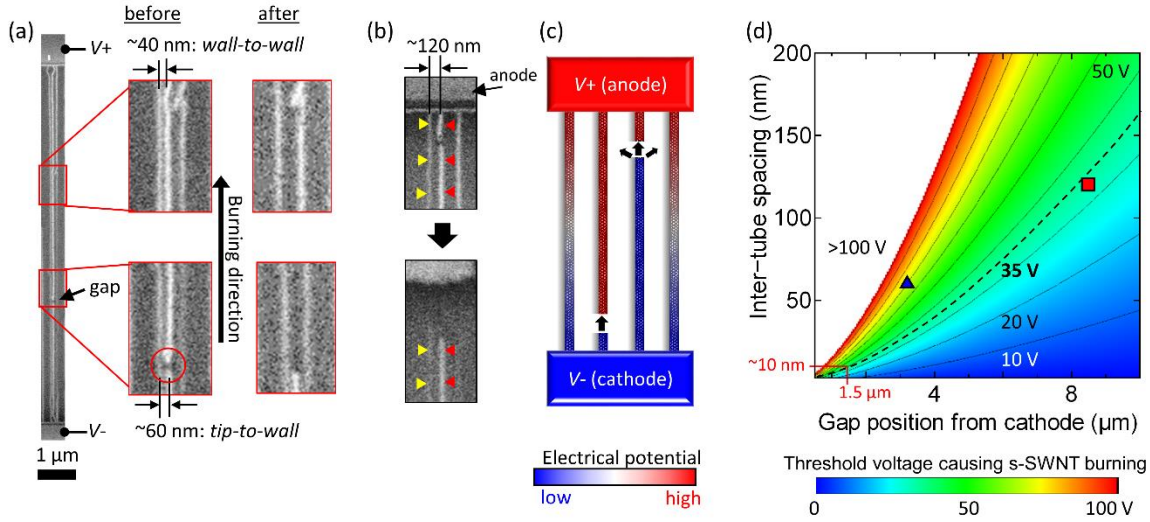


Figure 6 (a) SEM image of three parallel SWNTs after gap formation by electrical breakdown of the middle SWNT. Enlarged images of two regions before and after burning of the middle SWNT under WPA conditions by the application of 50 V are also shown. s-SWNTs were kept intact, though the minimum tip-to-wall and wall-to-wall distance in these SWNTs were 60 and 40 nm, respectively. (b) SEM images of s-SWNTs and an m-SWNT with a nanogap formed nearby the anode before (top) and after (bottom) the burning by the application of 40V. A neighboring s-SWNT was also burned. (c) Schematic of the electric potential for different gap positions (near anode or cathode). (d) Color contour plot of the calculated threshold voltage that unintentionally causes the burning of s-SWNTs, as a function of gap position (*x*-axis) and inter-tube spacing (*y*-axis). Two examples from (a) and (b) are plotted in a blue triangle and a red square, respectively.

CONCLUSIONS

We have demonstrated the fabrication of multiple transistors on a long purely s-SWNT array via the on-chip purification method. An s-SWNT array was obtained by selectively burning m-SWNTs in full length from as-grown aligned SWNTs with the assistance of water vapor and polymer coating. Since burning from site-controlled nanogaps can be triggered by the application of a relatively low voltage, there was negligible damage to s-SWNTs through the sorting. All the transistors fabricated along the purified array showed excellent switching behavior and larger on-state currents than those processed by electrical breakdown for scaled devices. The simple modeling of field enhancement at SWNT tips implied the applicability to the arrays with ~100 SWNTs/μm density, so that the sorting method could eventually lead to the upscaled integration of ultrascaled SWNT transistors for high-performance logic applications.

METHODS

SWNT growth and transfer. An r-cut quartz substrate was annealed at 900 °C in air, followed by the deposition of Fe catalyst (0.2 nm thick) by thermal evaporation in a selected area. After heating of the sample at 750 °C in air, horizontally aligned SWNTs were grown at 800 °C for 40 min with ethanol as a feedstock gas.[32,33] The SWNT arrays were transferred on the silicon substrates with the pre-patterned probing pads. Transfer of the SWNT arrays was achieved by a PMMA-mediated technique.[34] 4 wt% PMMA solution in anisole was spin-coated at 2000 rpm on the SWNTs. The substrates were heated at 170 °C in air for 15 min, and then immersed in heated aqueous KOH (1 mol/L, ~100 °C). The PMMA film was peeled off from the substrate in cold distilled water, and picked up by the silicon substrates. After

natural drying, the substrate was heated to 170 °C for 30 min. Finally, the PMMA films were removed by acetone rinsing and annealing in a buffer gas (Ar/H_2, 97/3%) at 350 °C for 150 min.

Probing pads and metal contacts. Probing pads and alignment markers (Ti/Pt, 1/24 nm) were deposited by sputtering on highly doped silicon substrates with 100-nm-thick oxide before the SWNT transfer step. The highly doped silicon served as a global back gate to modulate SWNT-based transistors. Unwanted SWNTs out of the active region were etched away by oxygen plasma. Au contacts (25 nm thick) were directly deposited onto the SWNT arrays by thermal evaporation. After the formation of nanogaps at controlled position by electrical breakdown in dry oxygen environment, another photolithography was performed to etch middle Au contacts with iodine-based gold etchant. Once the m-SWNTs in the active region were eliminated and all the Au contacts were etched away, electron-beam lithography was conducted to pattern small metal contacts (Ti/Au, 0.2/35 nm) for the fabrication of multiple transistors with relatively short channels along the s-SWNT array. Note that electrical measurements of transistors were performed in air at room temperature.

Selective burning of m-SWNTs. m-SWNTs were selectively removed by a water- and polymer-assisted burning method.[19] After forming nanogap in m-SWNTs and removing middle Au contacts, the SWNTs were embedded in a PMMA thin film (~26 nm thick) by spin-coating of 1 wt% PMMA ($M_W \approx 996{,}000$) solution in anisole. The SWNT sample was then placed in the chamber filled with a wet oxygen gas (O_2/H_2O, 90/2.4 kPa) at room temperature. The burning of m-SWNTs from the pre-formed nanogaps was initiated by

ramping the voltage from 0 to -35 V across the SWNTs, while positive gate voltage (V_{GS} = 10 V) was applied to preserve s-SWNTs. Here, negative voltage was applied to the bottom contacts (cathode), which were closer to the site-controlled nanogaps, because the burning from the nanogaps is propagated only in the same direction as electron flow.

ASSOCIATED CONTENT

Supporting Information. Details on purification and device fabrication processes, observation of a single m-SWNT burned from a nanogap, and analysis of short-channel devices on a single SWNT. This material is available free of charge via the Internet at heep://pubs.acs.org.

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ACKNOWLEDGEMENTS

Part of this work was financially supported by Kakenhi Grants-in-Aid (Nos. JP15H05760, JP25107002, JP17K06187, and JP17K14601) from the Japan Society for the Promotion of Science (JSPS). This work was partly conducted at the Center for Nano Lithography & Analysis and the VLSI Design and Education Center (VDEC). K.O. was financially supported by a JSPS Fellowship (JP15J07857).

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