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Facile Fabrication of All-SWNT Field-Effect Transistors

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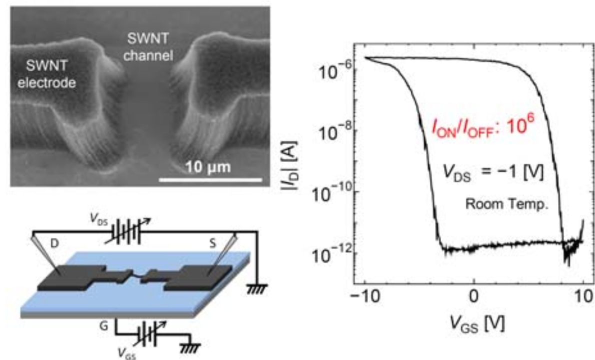

We fabricated field-effect transistors (FETs) using as-grown single-walled carbon nanotubes for the channel as well as both electrodes. The resulting FETs exhibited I_{ON}/I_{OFF} ratios exceeding 10^6 and a maximum ON-state current of more than 13 μA.

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ABSTRACT

We fabricated field-effect transistors (FETs) using as-grown single-walled carbon nanotubes (SWNTs) for the channel as well as both source and drain electrodes. The underlying Si substrate was employing as the back-gate electrode. Fabrication consisted of patterned catalyst deposition by surface modification followed by dip-coating and synthesis of SWNTs by alcohol chemical vapor deposition (CVD). The electrodes and channel were grown simultaneously in one CVD process. The resulting FETs exhibit excellent performance, with an I_{ON}/I_{OFF} ratio of 10^6 and a maximum ON-state current (I_{ON}) exceeding 13 μA. The large I_{ON} is attributed to SWNT bundles connecting the SWNT channel with the SWNT electrodes. Bundling creates a large contact area, which results in a small contact resistance despite the presence of Schottky barriers at metallic-semiconducting interfaces. The approach described here demonstrates a significant step toward the realization of metal-free electronics.

KEYWORDS

Single-walled carbon nanotube, Field-effect transistor, Patterned synthesis, Self-assembled monolayer, Schottky barrier, Interfacial dipole

1. Introduction

Very impressive numbers have been reported for carbon nanotube field-effect transistors (CNT-FETs), particularly those utilizing a single-walled carbon nanotube (SWNT) as the channel. With a field-effect mobility as high as 79,000 cm² V⁻¹ s⁻¹ [1], an I_{ON}/I_{OFF} ratio of more than 10^6 [2], a very low subthreshold slope of 60 mV/decade [3-5], and quasi-ballistic transport in short channels [6], SWNTs are one of the

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most attractive materials for future electronic applications [7,8]. Fabrication of devices that exhibit properties of single-channel CNT-FETs, however, is complicated and time-consuming. In addition, the maximum ON-state current (I_{ON}) is limited in several μA, which is significantly low. The I_{ON} can be increased by using a two-dimensional random network SWNT channel [9], but this would sacrifice the interesting properties that arise from the one-dimensional SWNT structure.

Kocabas *et al*. fabricated FETs employing source and drain electrodes consisting of random SWNT networks and horizontally aligned SWNT channels in a single chemical vapor deposition (CVD) step [10]. They achieved an I_{ON}/I_{OFF} ratio of ~10^3, but the relatively small (sub-μA) I_{ON} is possibly due to the low-density SWNT electrode, which provides higher sheet resistance. Recently, FETs utilizing CNTs as both electrodes and channel were also realized by Zhou *et al*. [11]. They demonstrated this using two CVD steps, synthesizing vertically aligned CNT electrodes in the first step, followed by horizontally aligned SWNTs to act as FET channels in a second step. Due to the large number of SWNT channels the performance achieved thus far is considerably lower than required for feasible FETs but these simple approaches have high practicability. Furthermore, such all-CNT devices will conceivably be flexible without degradation of their electrical properties [12,13], and are promising for the realization of metal-free electronics.

The use of CNTs as electrodes is expected to provide good contact with an SWNT channel [14,15]. In the case of graphene electrodes, excellent electrical contact to the SWNT channels can be achieved because their atomic structures are essentially the same [16]. Kaskela *et al*. also reported that the sheet resistance of an SWNT film can be decreased by increasing the length of SWNT bundles because of the large contact area [17]. If a bundle is formed between the SWNT channel and SWNT electrode, the contact resistance can be reduced and the output current should increase. Another advantage for the use of CNT electrodes is that established techniques for patterned growth of CNTs [18-21] will be directly available for electronic device fabrication.

Here we describe an all-SWNT FET fabrication process by which vertically aligned SWNT (VA-SWNT) electrode structures and in-plane SWNT channels can be simultaneously synthesized in one CVD process on a Si substrate acting as the back-gate electrode. The electrical properties of the as-grown SWNT-FETs could be immediately characterized, with no post-processing required, and exhibited I_{ON} exceeding 10 μA with I_{ON}/I_{OFF} ratios of more than 10^6.

2. Results and discussion

2.1 Device Fabrication

We recently reported site-selective growth of SWNTs by fabricating hydrophobic and hydrophilic regions on a Si substrate using a self-assembled monolayer (SAM) [22]. Although SWNTs can be locally synthesized for device fabrication by conventional lithography techniques [23,24], such procedures require many steps and catalyst materials are limited to those compatible with a dry deposition process. Our novel method eliminates the development and lift-off steps [22], and is an easily scalable wet method for localized catalyst deposition. Furthermore, dip-coating is considerably simpler and more cost-effective than electron beam evaporation or other vacuum deposition methods. In this study, we modified this liquid-based catalyst deposition method to pattern electrode structures, from which VA-SWNT electrodes and in-plane SWNT channels were simultaneously grown.

The fabrication scheme is illustrated in Fig. 1. A thermally oxidized *p*-type Si substrate (t_{ox}: 50 nm) was subjected to oxygen plasma to obtain a clean, hydrophilic surface. This was then submerged into an octadecyltrichlorosilane (OTS)/toluene solution to form an OTS-SAM. A positive-type photoresist (AZ P4400) was spin-coated onto the hydrophobic SAM, which was then patterned by standard photolithography processes (exposure and development). To remove the SAM in the exposed areas, descumming (100 W, 100 Pa) was performed for 3 min, after which the substrate was washed by acetone and isopropyl alcohol to dissolve any residual resist. The result was a Si substrate with precisely patterned hydrophobic and hydrophilic regions. Catalyst was loaded onto the hydrophilic areas of the patterned substrate by dip-coating, and

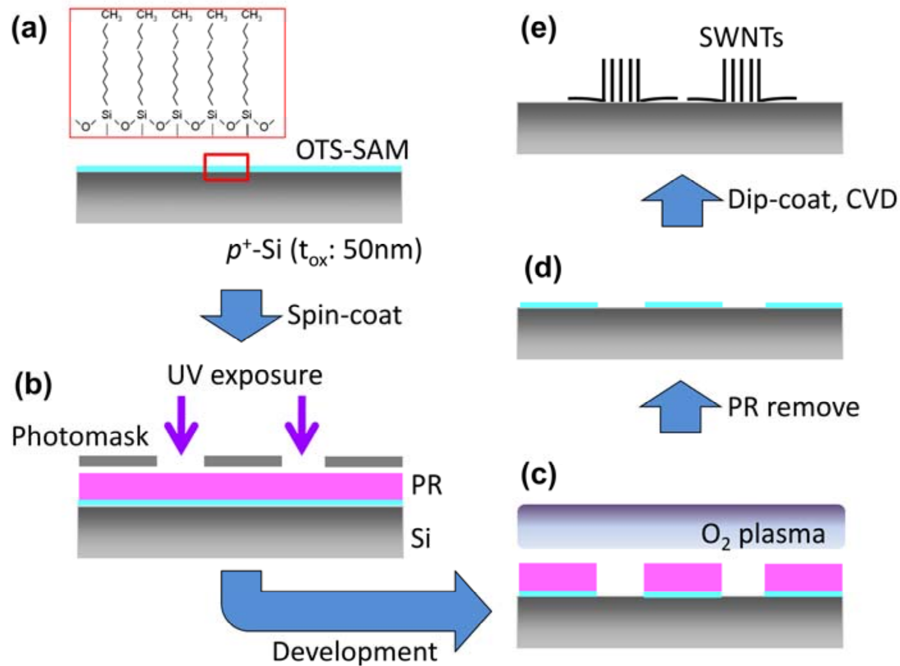

Figure 1 Process steps for all-SWNT FET fabrication: (a) Octadecyltrichrolosilane self-assembled monolayer (OTS-SAM) is formed on an oxidized Si substrate (t_{ox}: 50 nm); (b) photoresist is spin-coated onto the SAM and patterned by photolithography; (c) SAM is selectively removed by exposure to oxygen plasma; (d) removal of photoresist by acetone reveals patterned hydrophobic and hydrophilic regions on the substrate; (e) catalyst is selectively loaded onto hydrophilic regions by dip-coating, and SWNTs are obtained in these regions after synthesis by alcohol CVD.

SWNTs were synthesized by the typical alcohol CVD process [25-29]. Details regarding the experimental procedure are described in the last section.

SEM images of the resulting SWNT-FETs are shown in Fig. 2. The dark regions in Fig. 2(a) correspond to regions in which the SAM was removed by exposure to oxygen plasma. One of these regions is shown in the inset. The well-defined electrodes consist of VA-SWNTs, and are connected by one or two SWNTs crossing the channel [Fig. 2(b)]. Switchable current paths are formed when these SWNTs are semiconducting, yet the OFF current is not depleted should these SWNTs happen to be metallic. The probability of forming a semiconducting channel is dependent on the channel dimensions. We obtained the best results for a 15 μm channel width and 5 μm channel length, but our sample size is still rather small. Part of the electrode occasionally appears to be broken [Fig. S-1 in the Electronic Supplementary Material (ESM)], however this is simply because the SWNTs in this region did not sustain vertical alignment. Such FETs perform normally due to sufficient electrical connection through the fallen SWNTs, demonstrating the liberal tolerances in this fabrication method. Additionally, using VA-SWNT films as the electrodes offers two advantages. Firstly, VA-CNT bundles can be potentially useful for via interconnects [30-32]. Secondly, since the VA-SWNT films provide a very high surface area, the carrier transport properties may be tunable by adsorbing different molecules. We also note that the device was deliberately made to be large, but decreasing the size of the electrodes could reduce the overall footprint.

Resonance Raman spectra from the all-SWNT FETs are shown in Fig. 3. Spectra obtained from the electrode region (blue/upper spectrum in Fig. 3) clearly indicate the presence of SWNTs, which are identified from the G-band near 1590 cm^{-1} and the radial breathing mode (RBM) peaks in the 100 to 300 cm^{-1} range. A weak D-band near 1350 cm^{-1} indicates that the SWNTs are of high quality [26]. Spectra obtained from SAM-covered regions (black/lower spectrum in Fig. 3) show no indications of SWNTs.

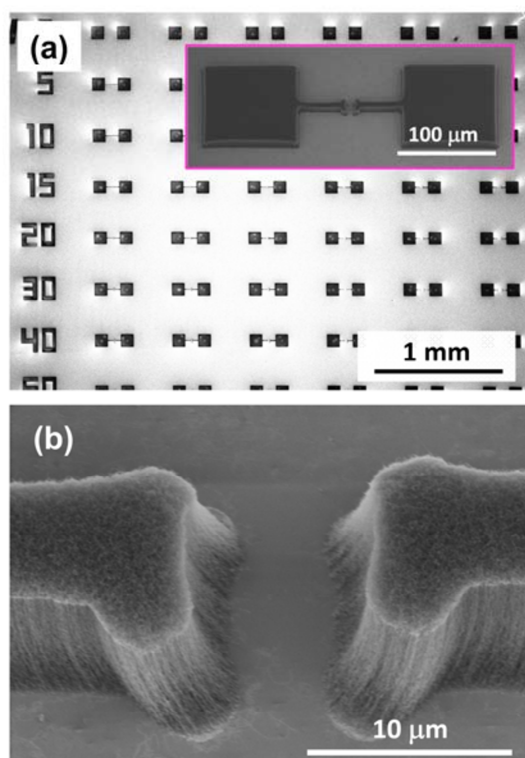

Figure 2 SEM images of (a) an array of all-SWNT FETs, and a SWNT-FET structure (magnified in inset). (b) The FET channel is formed by SWNTs on the surface, one or two of which make contact across the channel.

This is consistent with SEM observations (Fig. 2), which together demonstrate the efficacy of this technique for localized, site-selective SWNT synthesis. A sharp peak at 520 cm^{-1} (marked by an asterisk) is attributed to the silicon wafer substrate, and an artifact from the excitation laser (also marked) is found near 100 cm^{-1}.

2.2 FET Characteristics

A schematic diagram of an all-SWNT FET is shown in Fig. 4(a). To characterize the fabricated devices, probes were directly contacted to the VA-SWNT arrays acting as source and drain electrodes. The contact resistance (R_C) between the probe and the electrode is negligible because the contact area is considerably larger than that between the metallic VA-SWNT electrode array and the semiconducting SWNT channel. In addition, electrical conductance between SWNTs is dominated by resistance at SWNT-SWNT junctions [33,34]. Furthermore, since as-grown SWNTs include metallic tubes, the contact between the probe and the VA-SWNT array should be a low-resistance metallic-metallic (MM) connection rather than a metallic-semiconducting (MS) junction. This is discussed in more detail later. We note that attempting to short the probes by placing them on the same SWNT electrode resulted in a two-terminal resistance of several kΩ (Fig. S-2 in the ESM), which is much lower than the series resistance of the devices. The sheet resistance, however, is estimated to be much higher than conventional metal electrodes. We believe this can be reduced by chemical treatment [34,35], densification of the VA-SWNT electrodes [36] or use of another

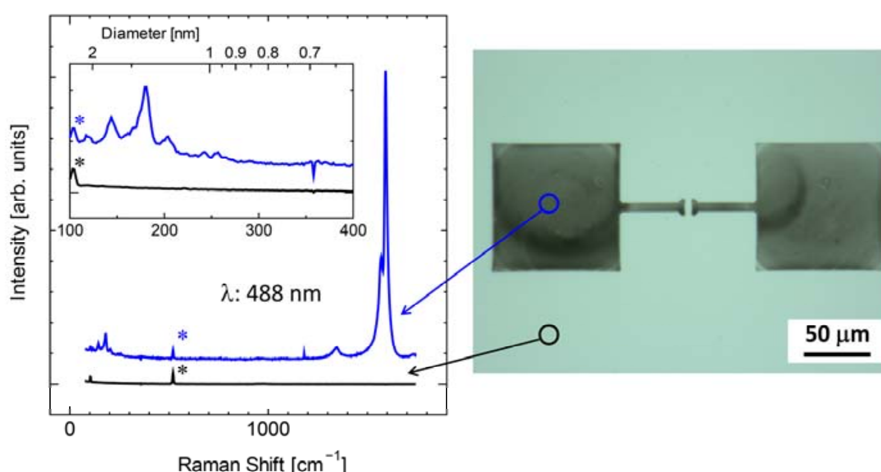

Figure 3 Raman spectra obtained from the substrate regions where OTS had been removed (upper/blue line) and remained (lower/black line). RBM peaks are shown in the inset (excitation wavelength, 488 nm). Measurement locations are indicated on the optical image.

CVD technique [17].

A SEM image of the measured device (15 μm channel width, 5 μm channel length) is shown in Fig. 4(b). Based on the measured properties, we believe that the channel is formed by one nanotube contact between the electrodes. If this were not the case, the linear-scale transfer characteristics (Fig. S-3 in the ESM) should not be smooth, due to the different threshold voltages that depend on the different SWNT band-gaps. Typical *p*-type semiconducting properties were measured for this device, as shown in Figures 4(c) and 4(d). The output characteristics (I_D-V_{DS}) indicate the maximum I_{ON} reached -13 μA at V_{DS} = -10 V. The saturation I_{ON} is as good as ohmically Pd-contacted CNT-FETs [7], however the ON-state resistance (R_{ON}) is estimated to be ~370 kΩ, which is 10 times higher than for Pd-contacted devices. This difference is attributed to Schottky barriers at MS SWNT junctions [33]. As the highest reported I_{ON} is approximately 4 μA for a Schottky barrier CNT-FET [37,38], the energy barrier limits electrical conductivity in the ON-state. The electrical conductance of our devices ($0.07e^2/h$) would otherwise be much greater than that of a cross-linked MS junction [33], despite being obtained by a two-terminal measurement (conductance is generally underestimated using the two-terminal method).

One possible reason our device allows such a large I_{ON} is that the SWNT channel forms a bundle in the electrode region. Bundling is due to van der Waals interactions with other nanotubes [39,40], which involve large surface areas, thus reducing the contact resistance between SWNTs. It may be possible to reduce the contact resistance by increasing the extent of bundling, but this has not yet been attempted. Another possible explanation for the high current may be due to the use of as-grown SWNTs. The fabrication process reported here

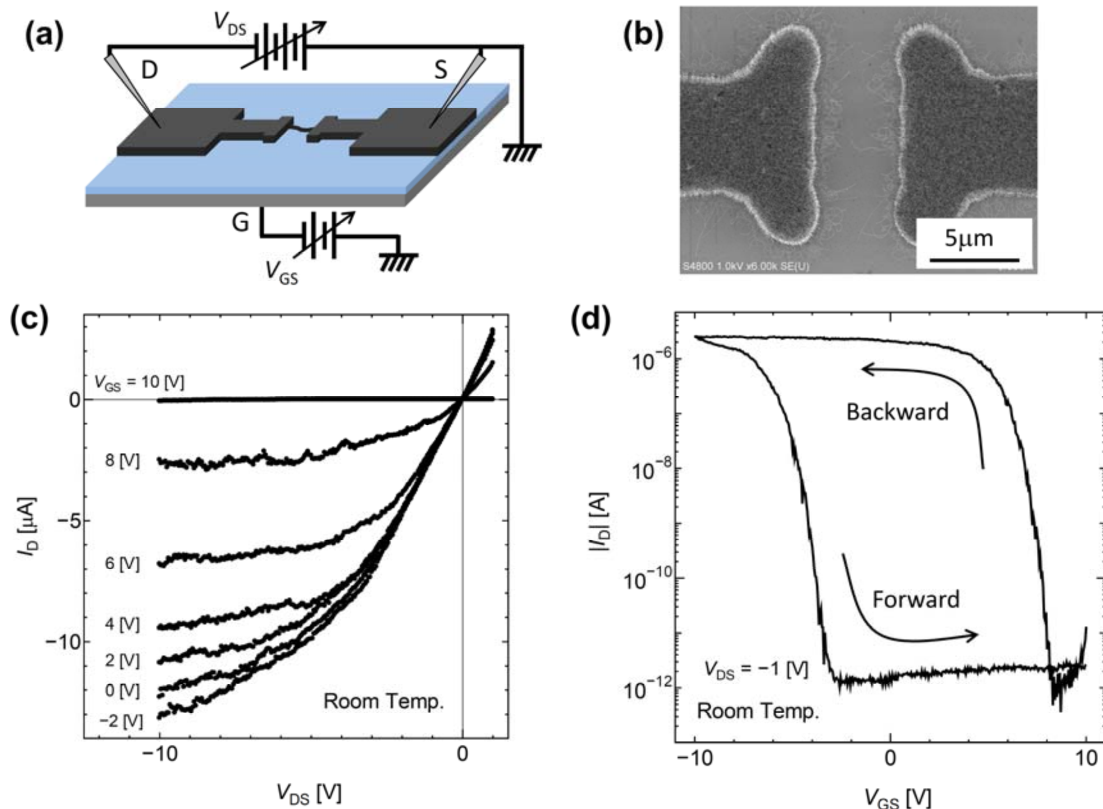

Figure 4 Electrical characteristics of a typical all-SWNT FET: (a) Schematic diagram of a back-gated all-SWNT FET measurement; (b) corresponding SEM image of a characterized device with channel length of 5 μm and electrode width of 15 μm; (c) output characteristics of the device, which was operated at room temperature under ambient conditions. V_{GS} was applied from +10 V to -2 V with a -2 V step. The ON-state resistance (R_{ON}) is ~370 kΩ; (d) transfer characteristics of the same device taken at V_{DS} = -1 V. The I_{ON}/I_{OFF} ratio is 10^6 and the subthreshold slope is 350 mV/decade.

includes no post-processing, essentially eliminating potential causes of damage to the SWNTs.

To summarize the transport characteristics: (i) R_{ON} is higher than in ohmically Pd-contacted CNT-FETs due to the presence of a Schottky barrier. However, (ii) our all-SWNT FETs show a large ON-state conductance (G_{ON}) compared with typical Schottky barrier CNT-FETs because of the large contact area between bundled SWNTs.

The transfer characteristics (I_D-V_{GS}) of our devices also show the I_{ON}/I_{OFF} ratio is more than 6 orders of magnitude at V_{DS} = -1 V, with a subthreshold slope ($S = \partial V_{GS}/\partial \log I_D$) of ~350 mV/decade and a transconductance ($g_m = \partial I_D/\partial V_{GS}$) of 1.21 μS (Fig. S-3 in the ESM). These values of S and g_m are quite low even though the maximum I_{ON} is relatively high, which may be due to the aforementioned Schottky barrier. In addition, hysteresis is observed in the forward (V_{GS}: -10 to +10 V) and backward (V_{GS}: +10 to -10 V) scan directions. We measured a slight current flow near V_{GS} = +10 V of the backward sweep, and the ambipolar characteristics appeared only when the gate voltage was swept from positive to negative. This electron injection into the SWNT channel is believed to be due to charge trapping at the substrate surface. When a positive back-gate bias is applied, negative charges are induced at the interface between the source and the oxide layer, which could lead to electron injection into the conduction band of the channel. Positive charges are similarly induced while in the negative bias regime on the forward sweep, but their contribution is significantly lower because trapped electrons at the interface at $V_{GS} > 0$ would be recombined with initially induced positive charges.

To demonstrate the advantage of our dip-coating method, we compare our all-SWNT FETs to conventional FETs fabricated using the same materials and identical SWNT synthesis conditions. Characterization of the SWNTs by SEM (Fig. S-4 in the ESM) and resonance Raman spectroscopy (Fig. S-5 in the ESM) indicate the SWNTs were very similar to those grown from dip-coated catalyst. Details on fabrication procedures and device performance can be found in the ESM. Unlike the all-SWNT FET, the conventionally fabricated FET showed considerable leak current at V_{DS} = 0 V [Fig. S-6(a) in the ESM], despite the same oxide layer thickness of 50 nm. The primary difference between these two fabrication methods is the amount of metal deposited on the substrate (which is considerably more in the case of conventional fabrication). The significant leak current is suspected to be caused by metal migration into the substrate [41]. This could be prevented by reducing the amount of metal deposited, but controlling a metal layer less than 1 nm thick (which was used here) is very difficult using dry deposition methods. The dip-coating method used to fabricate the all-SWNT FET, however, is believed to deposit little more than a monolayer of metal on the surface, and the mobility of this metal is believed to be inhibited by interaction with coexisting metal oxides [42]. This comparison simultaneously demonstrates the difficulty of realizing metal-free FETs using conventional approaches and the feasibility if using the wet method reported here.

2.3 Inter-Nanotube Interfacial Structure

As briefly mentioned above, understanding of nanotube junctions is important in this study. According to the Schottky model (under ideal conditions, ignoring the existence of an interlayer gap) the Fermi level (E_F) of a SWNT electrode should be positioned at the mid-gap of the SWNT channel, as shown in Fig. 5(a). This is because the work functions of the SWNT channel and both SWNT electrodes are essentially the same (~4.8 eV) [43]. The transfer characteristics should therefore be ambipolar [44]. The results, however, show typical *p*-type unipolar characteristics (Fig. 4). This implies the existence of an interfacial dipole [44-46], which causes an abrupt potential drop at the interface between the SWNT electrodes and the SWNT channel [Fig. 5(b)]. Interfacial dipoles are usually caused by adsorption of oxygen or water molecules [44,45], and their presence is almost guaranteed because the measurements were performed in air under ambient conditions. This is also believed to be responsible for the considerable hysteresis [47] seen in Fig. 4(d). Such a shift of the SWNT electrode potentials may be useful for conversion of carrier transport to *n*-type conduction.

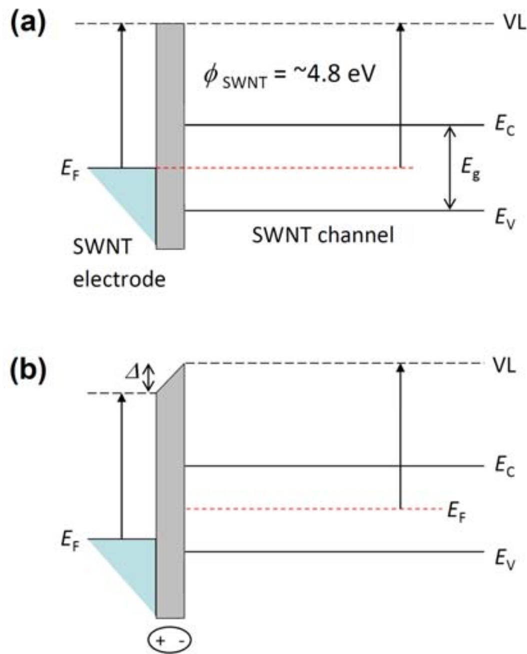

Figure 5 (a) An ideal interfacial diagram at the contact between SWNT electrode and SWNT channel. VL and E_F denote vacuum level and Fermi energy, while E_C and E_V indicate the conduction and valence band edges, respectively. (b) An interfacial diagram with a VL shift of Δ due to the presence of an interfacial dipole.

3. Conclusions

In conclusion, we have demonstrated simple fabrication of all-SWNT FETs utilizing catalyst localization by surface functionalization. The combination of a self-assembled monolayer with a standard photoresist was used to pattern precisely defined hydrophobic and hydrophilic regions on a substrate, which determined the location of dip-coated catalyst and thus SWNT growth. This approach is both simple and scalable, and is expected to afford a variety of all-SWNT devices in the future. We are also hopeful that all-SWNT devices, including the all-SWNT FETs presented here, could be the key to realizing future metal-free electronics.

Experimental

OTS-SAM Formation. A Si substrate was firstly subjected to oxygen plasma (100 W, 100 Pa) for ashing of organic contaminants, and was then immersed for 15 min in a toluene-OTS solution to form a hydrophobic SAM on the surface. The volumetric ratio of toluene to OTS was 500 to 1.

Catalyst Preparation and SWNT Synthesis. A Co/Mo acetate solution (0.01 wt% of each metal species dissolved in ethanol) was prepared for dip-coating. The patterned substrate was submerged into the solution for 1 min and was withdrawn at 4 cm/min. The catalyst was oxidized by annealing the dip-coated substrate in air at 400 °C, and was later reduced in a flowing Ar/H_2 mixture (3% H_2, 300 sccm flow rate, 40 kPa) during heating of the CVD chamber. When the chamber reached 800 °C, the Ar/H_2 flow was stopped and SWNTs were synthesized by supplying ethanol vapor at 1.3 kPa (10 Torr) for 10 min.

Device Characterization. After SWNT synthesis, the as-grown devices were characterized by a semiconductor parameter analyzer system (Agilent 4156C), resonance Raman spectroscopy (excitation wavelength, 488 nm), and scanning electron microscopy (SEM, acceleration voltage 1 kV). The Si substrate was used as a back-gate electrode for measuring the FET properties.

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Electronic Supplementary Material: Additional fabricated all-SWNT devices, sheet resistance estimate of VA-SWNT electrodes, additional FET properties, fabrication process of an all-SWNT FET

by conventional evaporation of Co thin film catalyst, SEM and Raman characterization of the synthesized SWNTs, and *I-V* characteristics of the resulting all-SWNT FET device are available in the online version of this article at http://dx.doi.org/10.1007/s12274-***-****-*.

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Electronic Supplementary Material

Facile Fabrication of All-SWNT Field-Effect Transistors

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Additional Fabricated All-SWNT Devices, Sheet Resistance Estimate of VA-SWNT Electrodes, and FET Properties

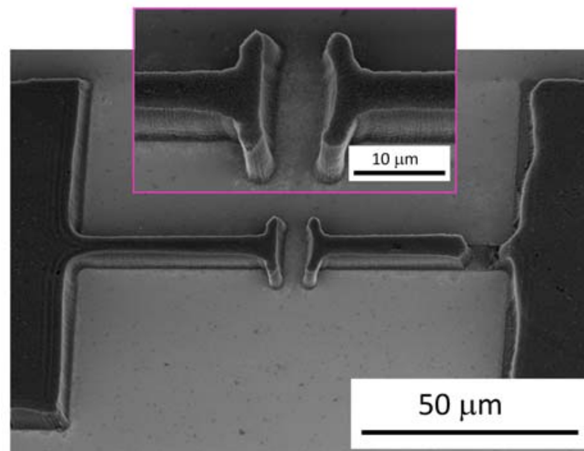

Figure S-1 Part of the electrode on the right side seems to be broken due to insufficient vertical alignment. This device, however, performed normally and exhibited FET characteristics.

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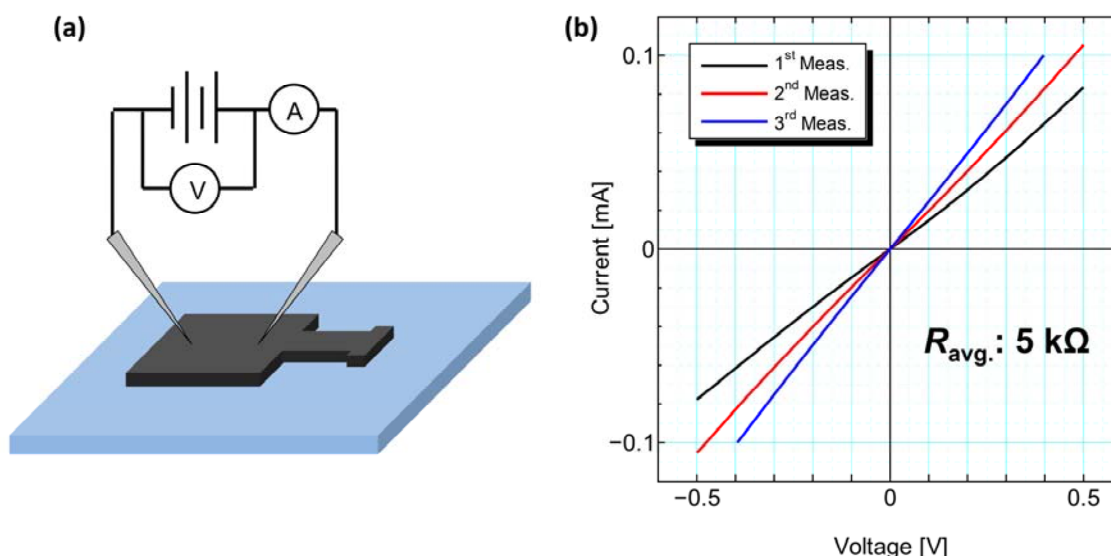

Figure S-2 Sheet resistance of an SWNT electrode by two-terminal measurement. (a) Schematic diagram of measurement setup. (b) The *I-V* curves denoted by 1st, 2nd, and 3rd were measured on different electrode pads. The average resistance is roughly estimated to be 5 kΩ.

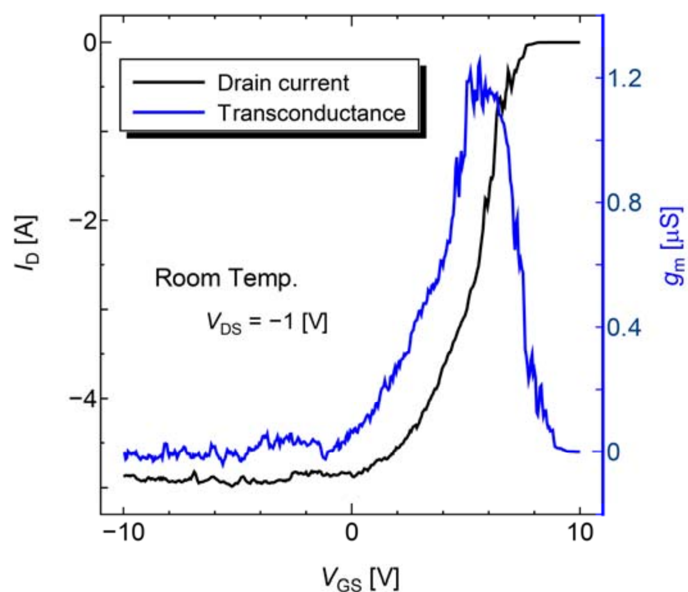

Figure S-3 Transfer characteristics (linear-scale) of the measured all-SWNT FET shown in Figure 4.

All-SWNT FET Fabricated by Evaporation of Co Thin-Film Catalyst

A thermally oxidized *p*-type Si wafer (t_{ox}: 50 nm) was used as a substrate. The catalyst pattern was made using a positive-type photoresist (AZ P4400), which was first spin-coated (4000 rpm, 40 s) over an adhesion layer of hexamethyldisilazane. UV exposure was performed for 8 s through the photomask after soft-bake (110 °C, 70 s). The substrate was soaked in 2.38% tetramethylammonium hydroxide (TMAH) for 3 min to

develop the exposed resist, and then followed by a hard-bake for 2 min at 120 °C. Residual resist in the pattern was removed by descuming (O_2: 100 Pa, RF: 100 W). The Co catalyst for SWNT growth was deposited as a thin film (thickness: 1 nm) using a thermal evaporator (ULVAC VPC-260F) with a quartz crystal thickness meter (CRTM-6000); excess metal was lifted off by dissolving the resist in acetone. After washing with isopropanol, the substrate was inserted into the CVD chamber for SWNT synthesis. The CVD conditions were the same as described in the main text. The Si substrate was used as a back-gate electrode for measuring *I-V* characteristics.

SEM and Raman Characterization

Patterned SWNT growth resulting from the above process is shown in Figure S-4(a). As has been demonstrated in many previous reports [S1-S4], this lithographic patterning obtained site-selective growth of CNTs. Figure S-4(b) shows that some SWNTs bridged the gap between the SWNT electrodes. Figure S-5 shows a resonance Raman spectrum from the SWNT area. A strong G-band (1590 cm^{-1}) and RBM peaks (100 – 300 cm^{-1}) confirm the presence of SWNTs.

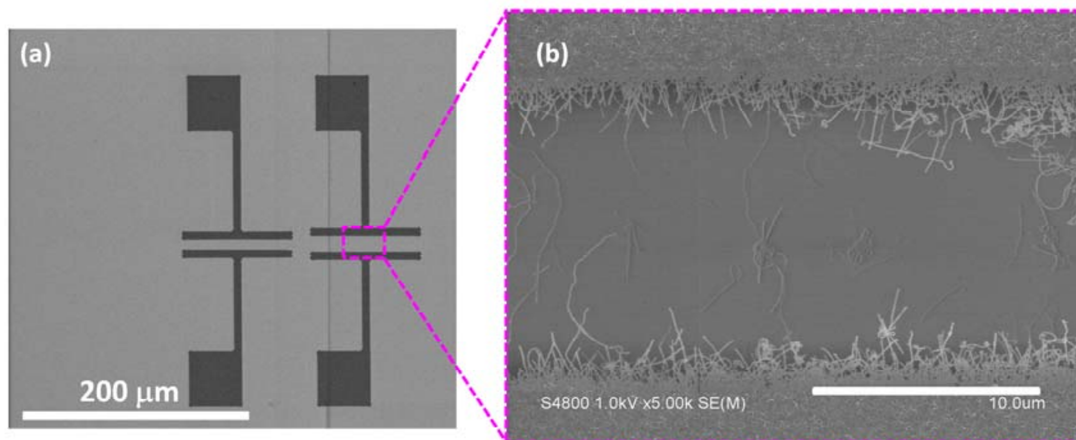

Figure S-4 SEM images of patterned growth of SWNTs from a deposited Co thin film: (a) Low magnification image of electrodes; (b) Magnification of the gap region in (a). Scale bar is 10 μm.

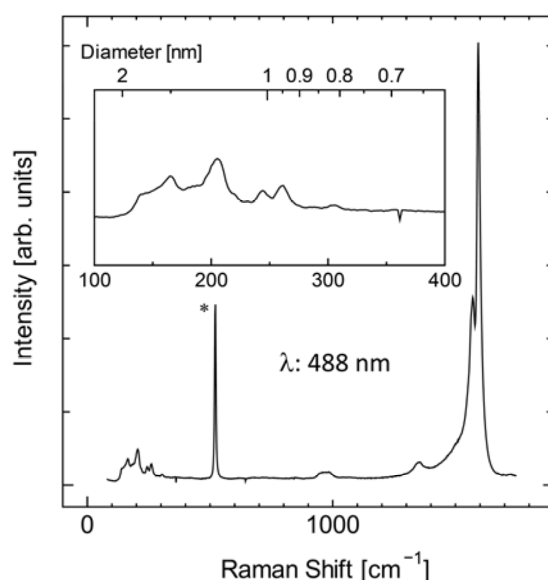

Figure S-5 Resonance Raman spectrum taken from the SWNT growth region in Figure S-3. RBM peaks, indicating the presence of SWNTs, are shown in the inset. The sharp peak near 500 cm^{-1} (marked by an asterisk) is due to bulk Si. The excitation wavelength is 488 nm.

I-V **Characteristics**

To measure the *I-V* properties, contact probes were directly approached to the SWNT pads and V_{DS} and V_{GS} were swept from +2.5 V to -2.5 V and from +10 V to -10 V respectively; a -2 V step was used in both cases. Figure S-6(a) shows a schematic cross-section diagram of an all-SWNT FET grown from a Co thin film. Output characteristics are shown in Figure S-6(b). A leak current was clearly observed at V_{DS} = 0 V for all measured devices. Despite the insulating nature of the SiO_2 layer, current from the drain (D) to the gate (G) was detected. In Figure S-6(c), the symmetric dependence of drain current (I_D) and the gate current (I_G) on V_{DS} indicate measurement of the same current flowing in opposite direction, hence the leak current is leaking through the oxide layer.

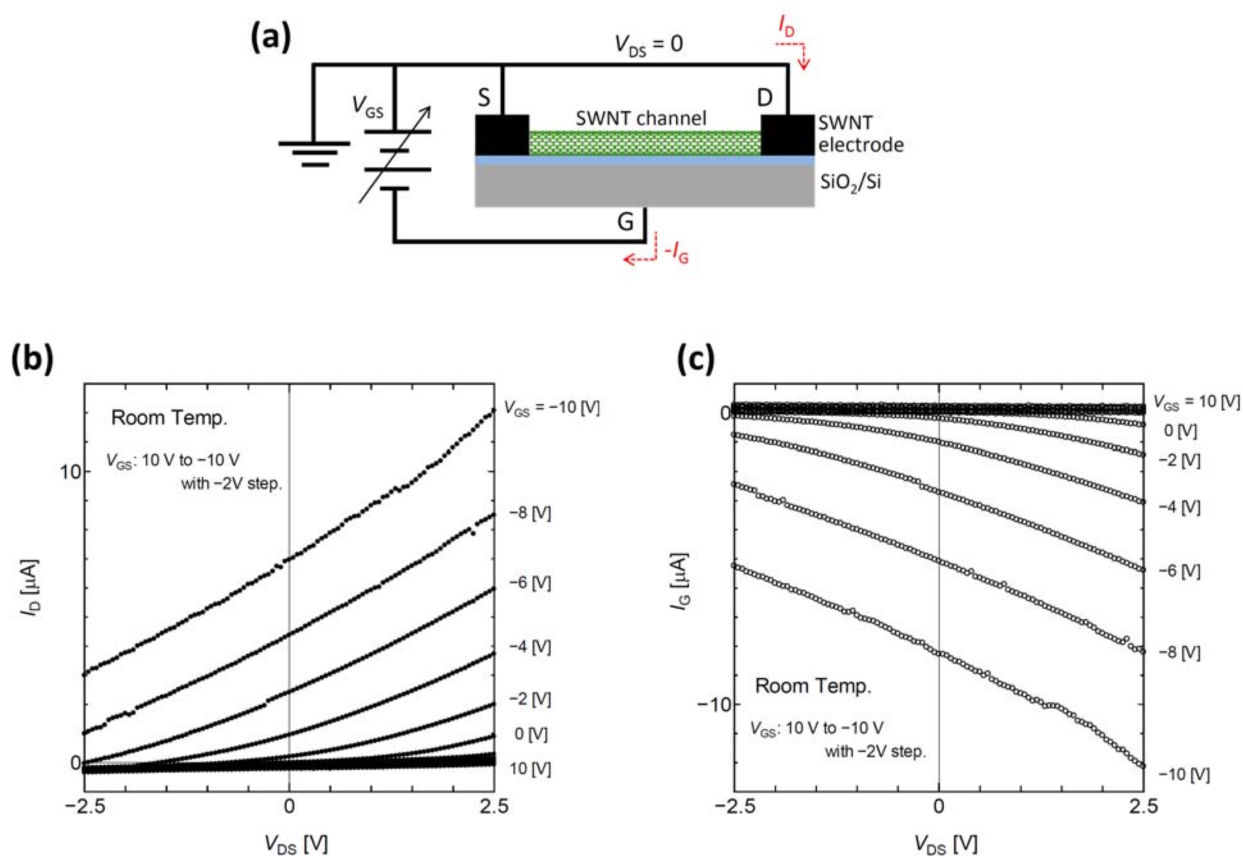

Figure S-6 Electrical characteristics of the all-SWNT FET synthesized from Co thin-film catalyst operated at ambient conditions: (a) Schematic diagram of the back-gated all-SWNT FET (V_{DS} = 0); (b) Output characteristics of the device. V_{GS} was applied from 10 V to -10 V with -2 V steps; (c) I_G vs. V_{DS} plot of the device.

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