Facile Fabrication and Characterization of a Field Effect Transistor using As-grown Single-Walled Carbon Nanotubes

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A single-walled carbon nanotube (SWNT) with small diameter (1-2 nm) is one of the most promising materials for application as an electron transporter, owing to its quasi one-dimensional structure. A carbon nanotube field effect transistor (CNT-FET) having an SWNT as its gate channel has been particularly investigated as a favorable nanoscale device for next-generation electronics [e.g., 1]. However, in most previous reports SWNTs were dispersed or transported during the device fabrication process, which may induce significant damage and/or doping of the SWNTs. A CNT-FET consisting of as-grown high-quality SWNTs may be obtained by depositing electrodes on as-grown SWNTs, but fabrication of fine structures (e.g., channel width < 1 μm) is still challenging.

Recently we succeeded in restricting the catalyst-coating area by patterning a self-assembled monolayer (SAM) on a Si substrate [2]. The growth location in this process can be precisely controlled down to 10 nm. This method has two primary advantages compared with conventional MEMS techniques (e.g., lift-off). Firstly, since the SAM surface is very hydrophobic it is possible to easily prepare substrates using a scalable liquid-based dip-coating method for catalyst deposition [3]. Secondly, the SAM can also be patterned with high resolution (~10 nm) using the electron beam of a scanning electron microscope (SEM), which makes the patterning process visible. A back-gate-type CNT-FET with an as-grown SWNT bridge and pre-deposited source and drain electrodes was fabricated using this method. The CNT-FET fabrication process is as follows. After SAM formation on a SiO_2/Si substrate with pre-patterned electrodes, the substrate was installed into a SEM to selectively remove the SAM using the electron beam. Catalyst was then deposited by dip-coating the substrate into a Co solution, and SWNTs were grown by ACCVD [4]. The *I-V* characteristics were measured using the Si substrate as a back-gate. Here we discuss the fabrication process and measured properties of the device.

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